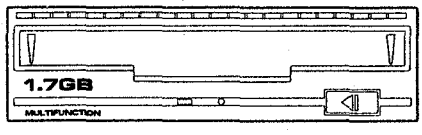
PIONEER®
The Art of Entertainment

Service Manual



ORDER NO.
RRV1269

OPTICAL DISK DRIVE UNIT

DE-UH9101

THIS MANUAL IS APPLICABLE TO THE FOLLOWING MODEL(S) AND TYPE(S).

Type	Model	Power Requirement	Remarks
	DE-UH9101		
ZUC/WL	○	DC power supply	

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1. SAFETY INFORMATION

This service manual is intended for qualified service technicians; it is not meant for the casual do-it-yourselfer. Qualified technicians have the necessary test equipment and tools, and have been trained to properly and safely repair complex products such as those covered by this manual.
Improperly performed repairs can adversely affect the safety and reliability of the product and may void the warranty. If you are not qualified to perform the repair of this product properly and safely, you should not risk trying to do so and refer the repair to a qualified service technician.

WARNING
Lead in solder used in this product is listed by the California Health and Welfare agency as a known reproductive toxicant which may cause birth defects or other reproductive harm (California Health & Safety Code, Section 25249.5).
When servicing or handling circuit boards and other components which contain lead in solder, avoid unprotected skin contact with the solder. Also, when soldering do not inhale any smoke or fumes produced.

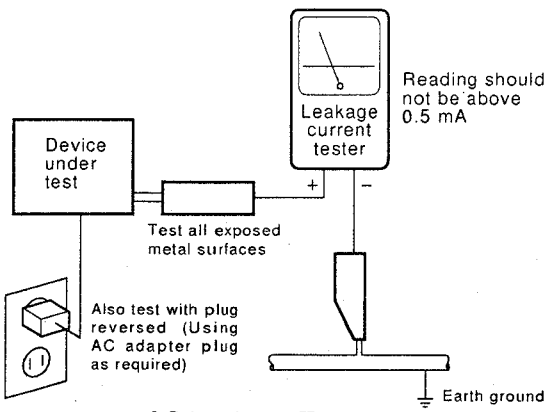
(FOR USA MODEL ONLY)

1. SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Measure leakage current to a known earth ground (water pipe, conduit, etc.) by connecting a leakage current tester such as Simpson Model 229-2 or equivalent between the earth ground and all exposed metal parts of the appliance (input/output terminals, screwheads, metal overlays, control shaft, etc.). Plug the AC line cord of the appliance directly into a 120V AC 60 Hz outlet and turn the AC power switch on. Any current measured must not exceed 0.5 mA.


Leakage current tester
Reading should not be above 0.5 mA
Device under test
+
–
Test all exposed metal surfaces
Also test with plug reversed (Using AC adapter plug as required)
Earth ground

AC Leakage Test

ANY MEASUREMENTS NOT WITHIN THE LIMITS OUTLINED ABOVE ARE INDICATIVE OF A POTENTIAL SHOCK HAZARD AND MUST BE CORRECTED BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

2. PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in the appliance have special safety related characteristics. These are often not evident from visual inspection nor the protection afforded by them necessarily can be obtained by using replacement components rated for voltage, wattage , etc. Replacement parts which have these special safety characteristics are identified in this Service Manual.

Electrical components having such features are identified by marking with a ⚠ on the schematics and on the parts list in this Service Manual.
The use of a substitute replacement component which dose not have the same safety characteristics as the PIONEER recommended replacement one, shown in the parts list in this Service Manual, may create shock, fire, or other hazards.

Product Safety is continuously under review and new instructions are issued from time to time. For the latest information, always consult the current PIONEER Service Manual. A subscription to, or additional copies of, PIONEER Service Manual may be obtained at a nominal charge from PIONEER.

(FOR EUROPEAN MODEL ONLY)

VARO !
AVATTAESSA JA SUOJALUKITUS OHITETTAESSA OLET ALTTIINA NÄKYMÄTTÖMÄLLE LASERSÄTEILYLLE. ÄLÄ KATSO SÄTEESEEN.

ADVERSEL:
USYNLIG LASERSTRÅLING VED ABNING NÅR SIKKERHEDSAFBRYDERE ER UDE AF FUNKTION UNDGÅ UDSAETTELSE FOR STRÅLING.

VARNING !
OSYNLIG LASERSTRÅLNING NÄR DENNA DEL ÄR ÖPPNAD OCH SPÄRREN ÄR URKOPPLAD. BETRAKTA EJ STRÅLEN.

LASER
Kuva 1
Lasersateilyn varoitusmerkki

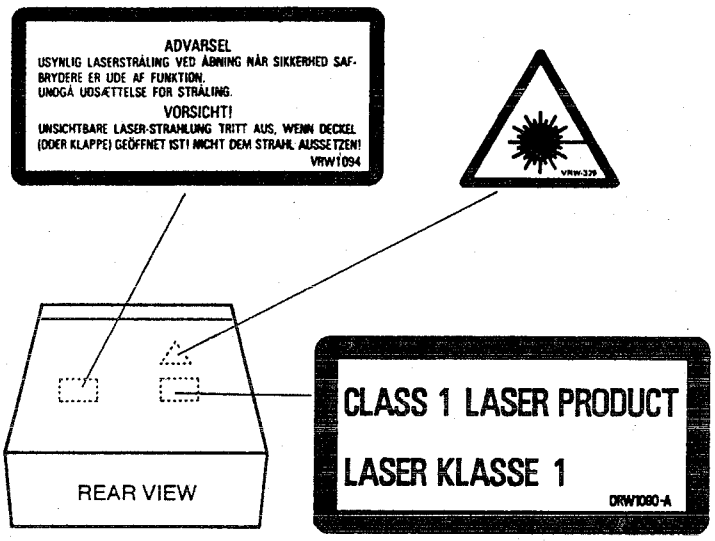
WARNING !
DEVICE INCLUDES LASER DIODE WHICH EMITS INVISIBLE INFRARED RADIATION WHICH IS DANGEROUS TO EYES. THERE IS A WARNING SIGN ACCORDING TO PICTURE 1 INSIDE THE DEVICE CLOSE TO THE LASER DIODE.

IMPORTANT
THIS PIONEER APPARATUS CONTAINS LASER OF CLASS 1.
SERVICING OPERATION OF THE APPARATUS SHOULD BE DONE BY A SPECIALLY INSTRUTED PERSON.

LASER DIODE CHARACTERISTICS
MAXIMUM OUTPUT POWER: 5 mw
WAVELENGTH: 780 - 785 nm

LASER
Picture 1
Warning sign for laser radiation

LABEL CHECK



Additional Laser Caution

1. Laser Interlock Mechanism
   The ON/OFF (ON : low level, OFF : high level) status of the D109 and S102 switches (Main board assy) for detecting the loading state is detected by the drive CPU, and the design prevents laser diode oscillation when both switches D109 and S102 are not OFF (high level) (clamped state).
   However, the interlock operates in the test mode*.

2. When the cover is opened, close viewing of the objective lens with the naked eye will cause exposure to a Class 1 laser beam.

* Refer to page 27.

2. EXPLODED VIEWS, PACKING AND PARTS LIST

NOTES :

- *Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*

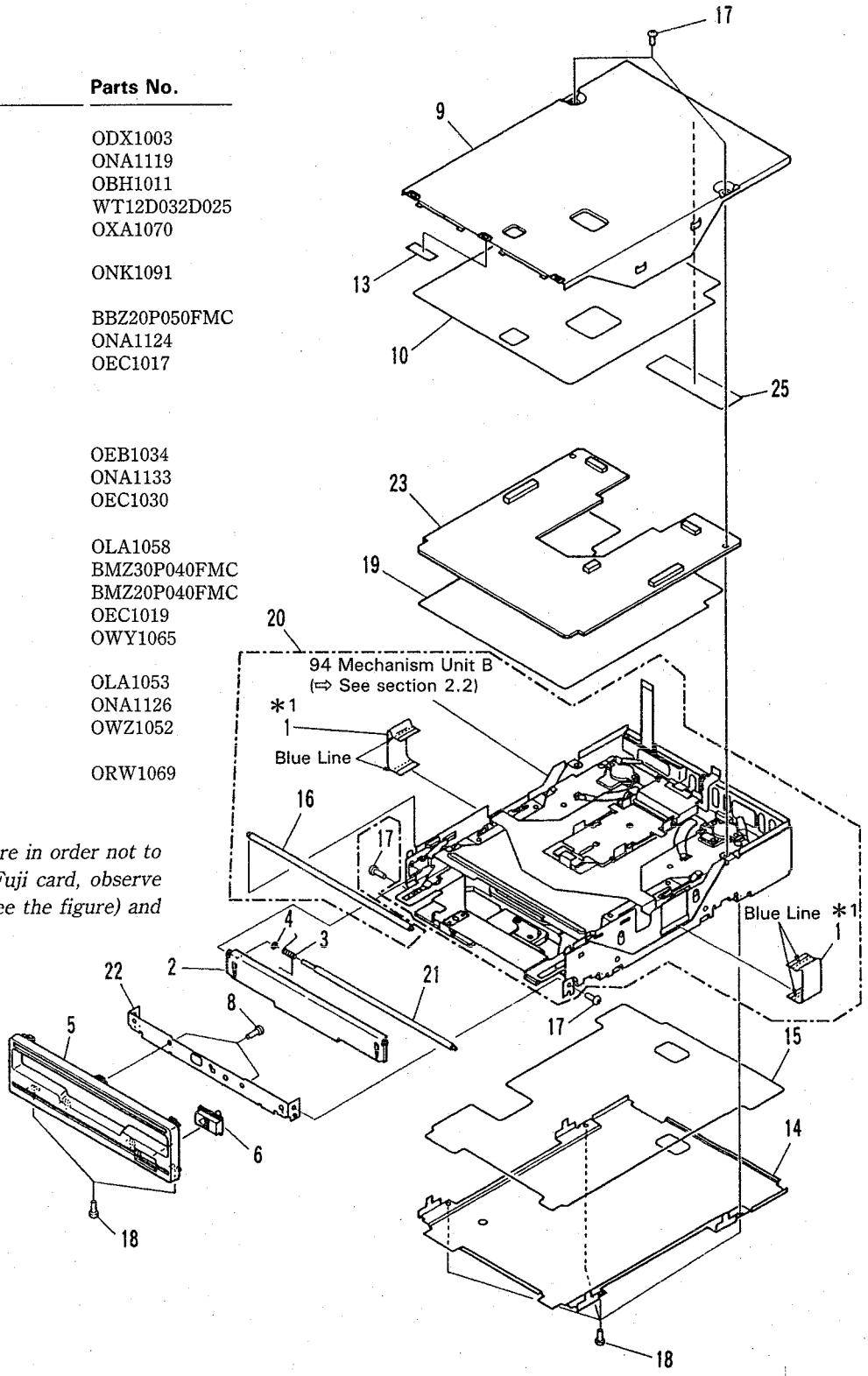
2.1 EXTERIOR

Parts List

Mark	No.	Description	Parts No.
*1	1	Fuji card/20P, 50MM	ODX1003
	2	Door	ONA1119
	3	Door sp	OBH1011
	4	Washer	WT12D032D025
	5	Front vessel assy	OXA1070
	6	E button	ONK1091
	7	.....	
	8	Screw	BBZ20P050FMC
	9	Top case	ONA1124
	10	Insulation sheet T	OEC1017
	11	.....	
	12	.....	
	13	STB pad	OEB1034
	14	Bottom plate	ONA1133
	15	Insulation sheet B	OEC1030
	16	STB bar	OLA1058
	17	Screw	BMZ30P040FMC
	18	Screw	BMZ20P040FMC
	19	Insulation sheet S	OEC1019
NSP	20	94 mechanism unit B	OWY1065
NSP	21	Door shaft	OLA1053
NSP	22	Front plate	ONA1126
NSP	23	94 servo board assy	OWZ1052
	24	.....	
NSP	25	65 label	ORW1069

Note:

**1; Handle the Fuji card with care in order not to break. When attaching the Fuji card, observe the blue lines on the card (see the figure) and firmly insert it to the end.*



2.2 94 MECHANISM UNIT B

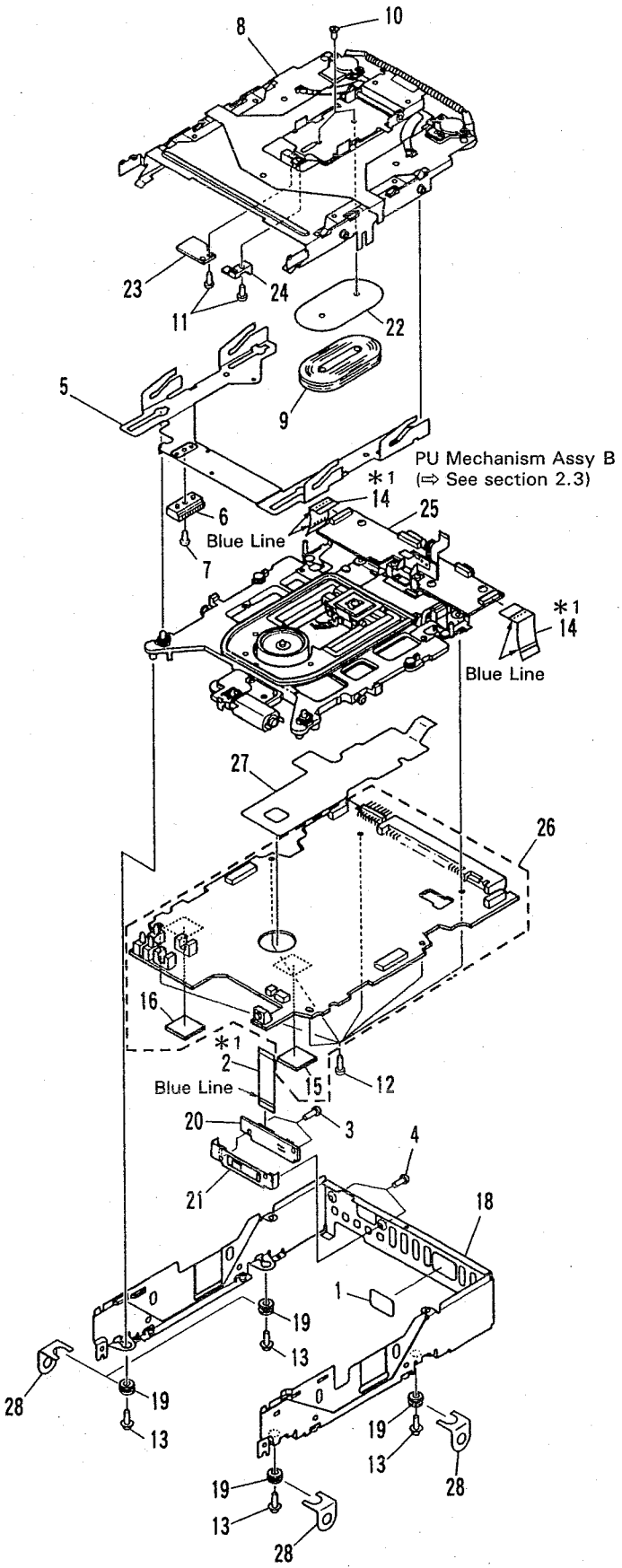
Parts List

Mark	No.	Description	Parts No.
	1	Blind	OEC1001
*1	2	Fuji card/08P, 44MM	ODX1005
	3	Screw	BMZ20P040FMC
	4	Screw	PMH20P040FMC
	5	S frame assy	OXA1062
	6	Rack	ONK1073
	7	Screw	PMA26P040FMC
	8	C holder unit	OXA1065
	9	BM coil assy	OTL1051
	10	Screw	UGZ20P080FNI
	11	Screw	JFZ20P030FNI
	12	Screw	BMZ30P040FMC
	13	Screw	AMZ30P080FMC
*1	14	Fuji card/10P, 25MM	ODX1002
	15	Drive CPU, IC (IC146)	PD3309A9
	16	Controller ROM, IC (IC333)	OYW1076
	17	.....	
NSP	18	Chassis	ONA1117
NSP	19	Insulator	OEB1028
NSP	20	94 Changer I/F board assy	OWZ1054
NSP	21	Divide PCB holder	ONA1129
NSP	22	BM sheet	OEC1027
NSP	23	94 BM connector board assy	OWZ1053
NSP	24	Disc guard	ONK1076
NSP	25	PU mechanism assy B	OWY1064
	26	Main board assy B	OEA1021
NSP	27	Slide guard sheet	OEC1035
NSP	28	Spring	OBK1034

Note:

**1; Handle the Fuji card with care in order not to break. When attaching the Fuji card, observe the blue lines on the card (see the figure) and firmly insert it to the end.*

NOTE: Screws adjacent to ▼ mark on the product are used for disassembly.



2.3 PU MECHANISM ASSY B

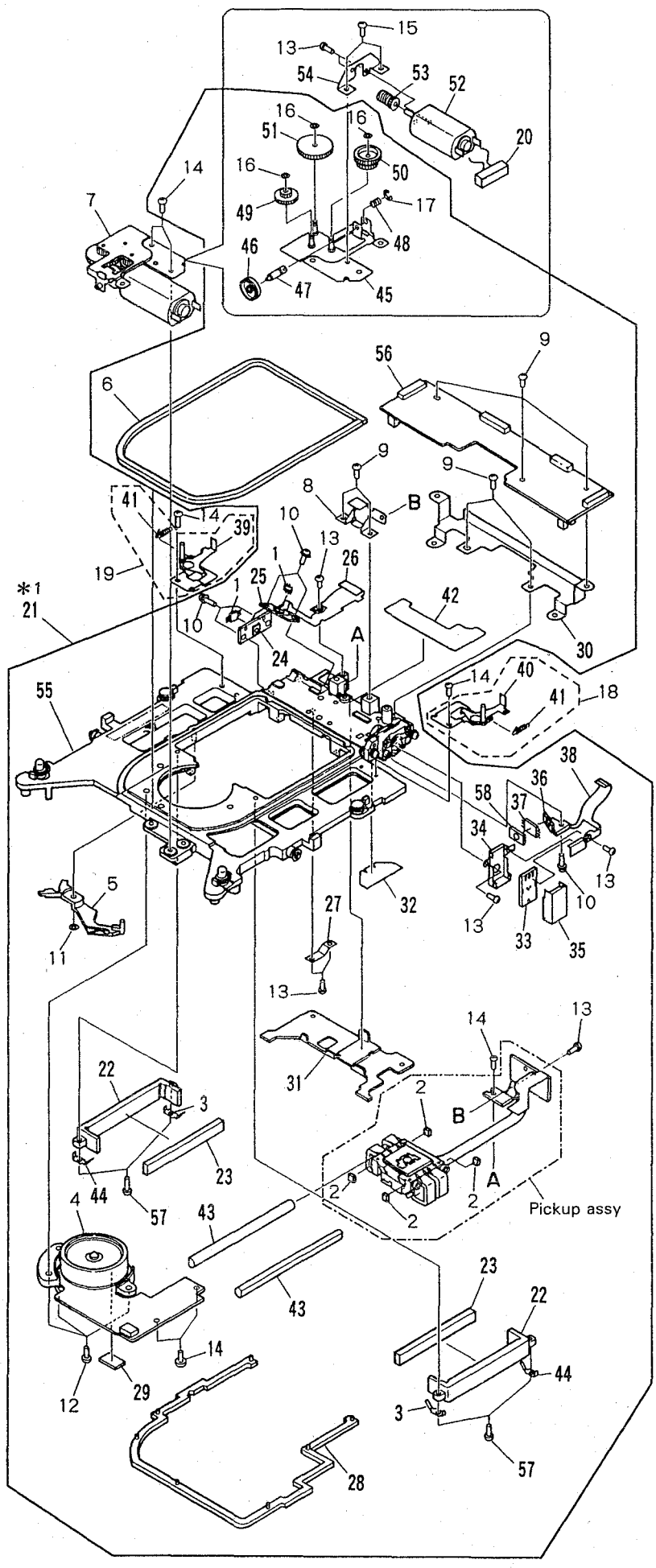
Parts List

Mark	No.	Description	Parts No.
NSP	1	Silicone photo diode	S2856−04
	2	Cushion	OEB1032
NSP	3	S spring R	OBK1033
	4	Spindle motor	OXM1015
	5	C lock arm	ONK1088
	6	Pad	OEB1036
	7	Loading drive assy	OWY1051
	8	BM support	ONA1125
	9	Screw	BMZ30P040FMC
	10	Screw	PMH20P060FMC
	11	Washer	WT26D047D050
	12	Screw	BMZ30P060FMC
	13	Screw	JFZ20P030FNI
	14	Screw	BMZ20P040FMC
	15	Screw	PMH20P040FMC
	16	Washer	WT16D032D050
	17	E ring	YE15FUC
	18	C sensor R unit	OWY1052
	19	C sensor L unit	OWY1055
	20	Connector assy	ODF1008
*1	21	Mechanism unit	OYM1032
NSP	22	C yoke	ONH1033
NSP	23	C magnet	OMF1010
NSP	24	PD holder A	ONA1103
NSP	25	PD holder B	ONA1104
NSP	26	PD flexible 130	ONP1077
NSP	27	Lens spring	OBK1024
NSP	28	Spacer	ONK1087
NSP	29	Spacer sheet	OEC1029
NSP	30	PCB support	ONA1122
NSP	31	PU cover assy	OXX1007
NSP	32	LD seal	OEC1022
NSP	33	94 OSC board assy	OWX1090
NSP	34	OSC case A	ONA1105
NSP	35	OSC case B	ONA1106
NSP	36	MD holder	ONK1061
NSP	37	PIN photo diode	PN3405N−SL
NSP	38	LD flexible 130	ONP1078
NSP	39	C sensor L assy	OXA1057
NSP	40	C sensor R assy	OXA1058
NSP	41	C sense SP	OBH1010
NSP	42	Cover sheet	OEC1038
NSP	43	C shaft	OLA1062
NSP	44	S spring L	OBK1032
NSP	45	Gear base assy	OXA1056

Mark	No.	Description	Parts No.
NSP	46	ME gear	ONK1075
NSP	47	ME shaft	OLA1054
NSP	48	MESP	OBH1009
NSP	49	Gear B	ONK1070
NSP	50	Gear A	ONK1069
NSP	51	Gear C	ONK1071
NSP	52	Motor	VXM1045
NSP	53	Worm	ONK1072
NSP	54	Motor bracket	ONA1121
NSP	55	PU frame assy	OXA1068
	56	PU board assy	OEA1020
	57	Screw	BMZ20P080FMC
NSP	58	PD mask	OEC1031

Note:

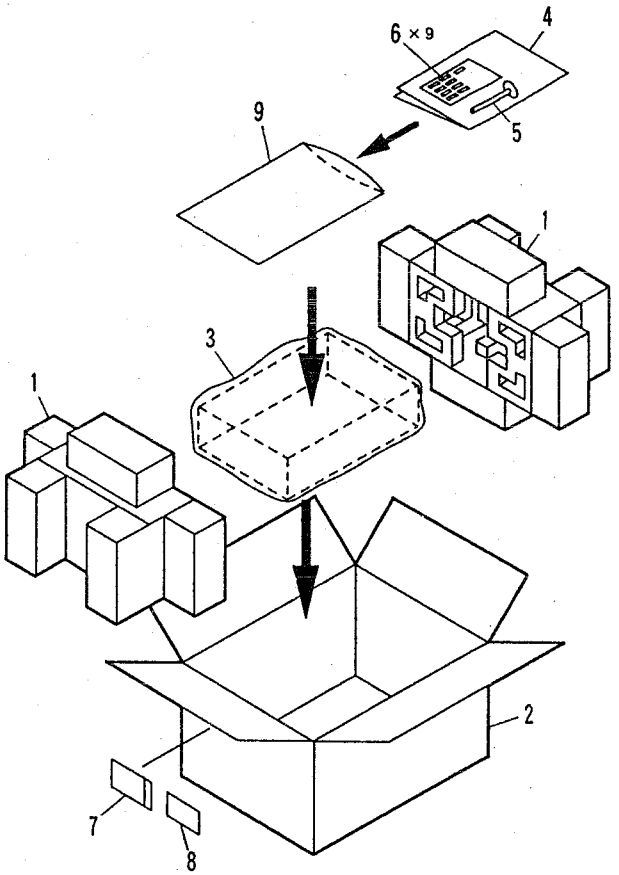
**1; The mechanism unit includes Rack, ONK1073 and S frame assy, OXA1062. (Refer to page 5.)*


Pickup assy

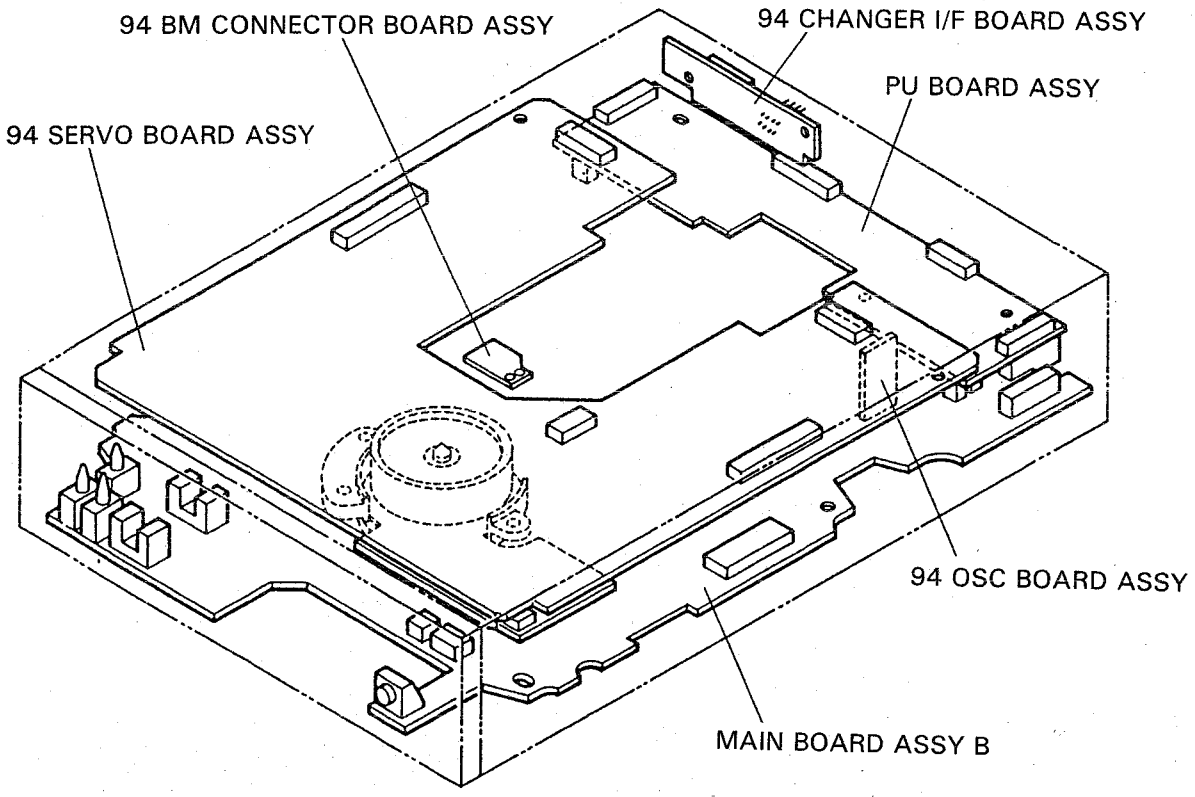
2.4 PACKING

Parts List

Mark	No.	Description	Parts No.
	1	Pad	OHA1029
	2	Packing case	OHG1102
	3	Packing bag	OHL1020
	4	Operating instructions (Japanese/English/French/ German)	ORM1056
	5	Screwdriver	NDV3
	6	Short pin	OKX1005
NSP	7	Follow card bag	DHL1011
NSP	8	Follow up card	DRY1032
NSP	9	Polyethylene bag	Z21−019



3. PCB LOCATIONS



4. SCHEMATIC DIAGRAMS

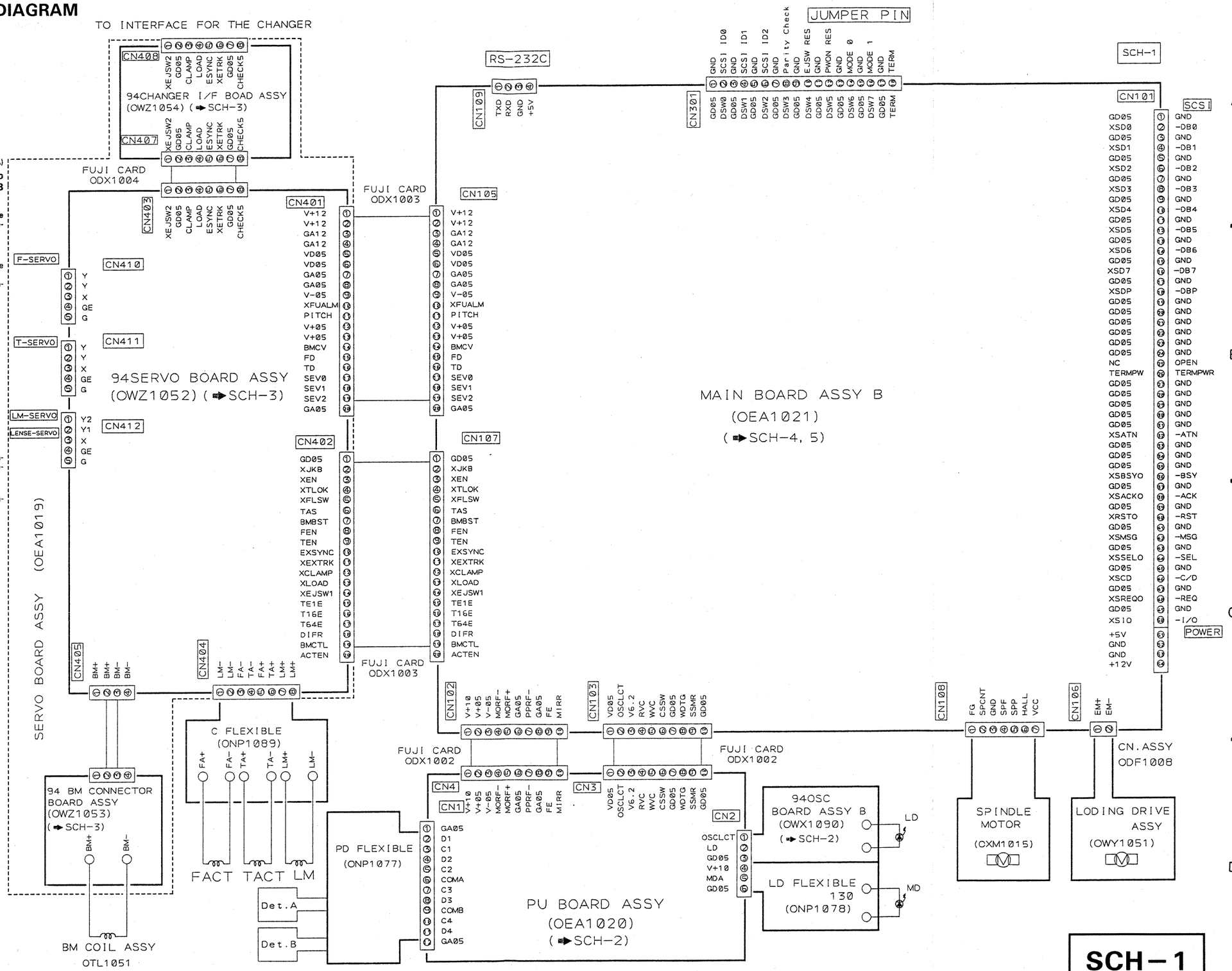
4.1 OVERALL SCHEMATIC DIAGRAM

NOTE FOR SCHEMATIC DIAGRAMS (Type 4A)

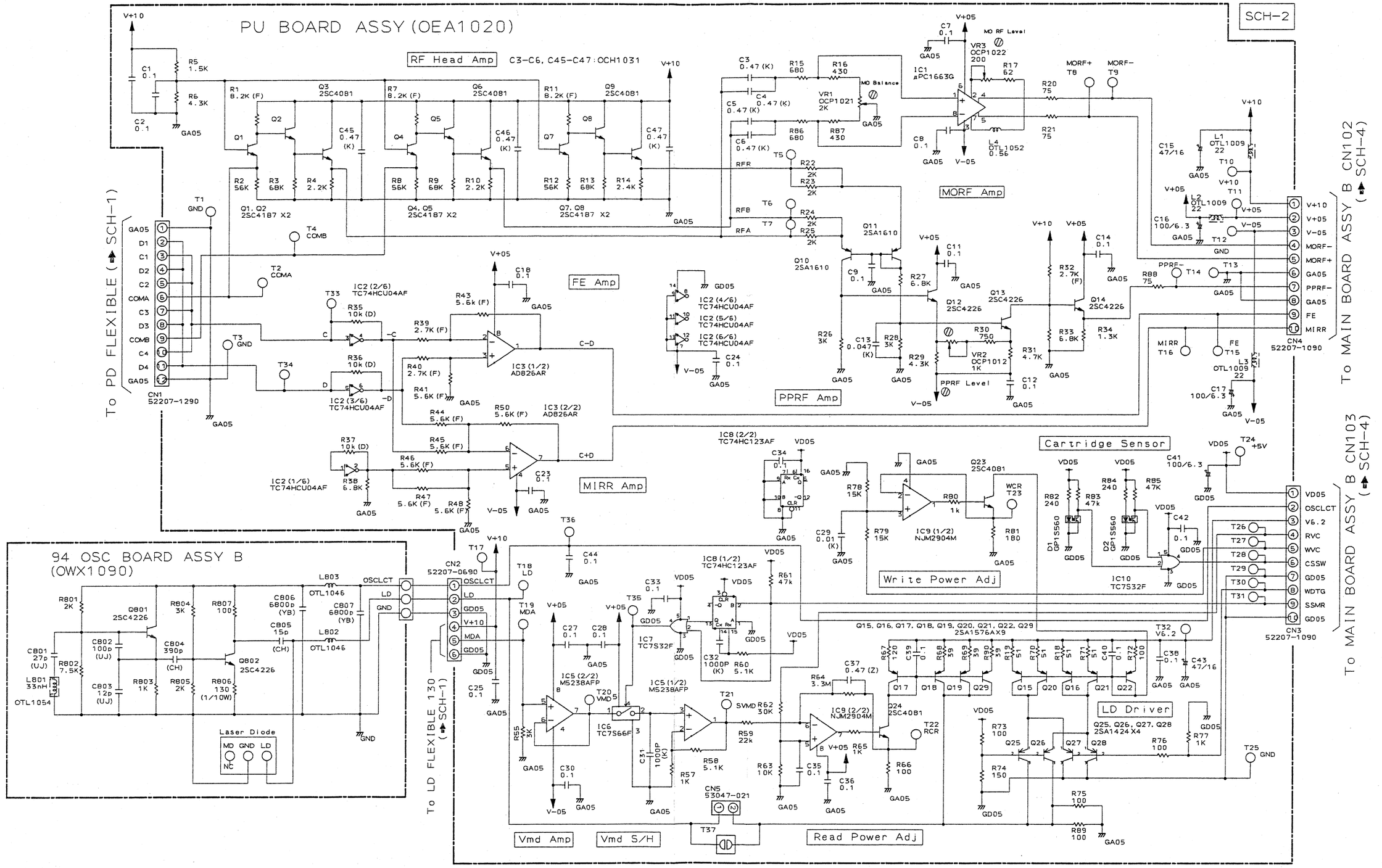
1. **When ordering service parts, be sure to refer to "PARTS LIST of EXPLODED VIEWS" or "PCB PARTS LIST".**
2. **Since these are basic circuits, some parts of them or the values of some components may be changed for improvement.**
3. **RESISTORS:**
   Unit: k:kΩ, M:MΩ, or Ω unless otherwise noted.
   Rated power: 1/4W, 1/6W, 1/8W, 1/10W unless otherwise noted.
   Tolerance: (F): ±1%, (G): ±2%, (K): ±10%, (M): ±20% or ±5% unless otherwise noted.
4. **CAPACITORS:**
   Unit: p:pF or μF unless otherwise noted.
   Ratings: capacitor (μF)/ voltage (V) unless otherwise noted.
   Rated voltage: 50V except for electrolytic capacitors.
5. **COILS:**
   Unit: m:mH or μH unless otherwise noted.
6. **VOLTAGE AND CURRENT:**
   ▭ or ← V :
   DC voltage (V) in PLAY mode unless otherwise noted.
   ⇦ mA or ← mA :
   DC current in PLAY mode unless otherwise noted.
   Value in ( ) is DC current in STOP mode.
7. **OTHERS:**
   - ⊘ or ❶ : Adjusting point.
   - ⋘ : Measurement point.
   - The ⚠ mark found on some component parts indicates the importance of the safety factor of the parts. Therefore, when replacing, be sure to use parts of identical designation.
8. **SCH—□ ON THE SCHEMATIC DIAGRAM:**
   - SCH—□ indicates the drawing number of the schematic diagram. (SCH stands for schematic diagram.)
9. **SWITCHES** (Underline indicates switch position):

MAIN BOARD ASSY B
S101 :EJECT
S102 :Carriage sense hole detector (Write protect)
S103 :Carriage sense hole detector (High reflectance)
S104 :Carriage sense hole detector (effective surface/ ineffective surface)*1

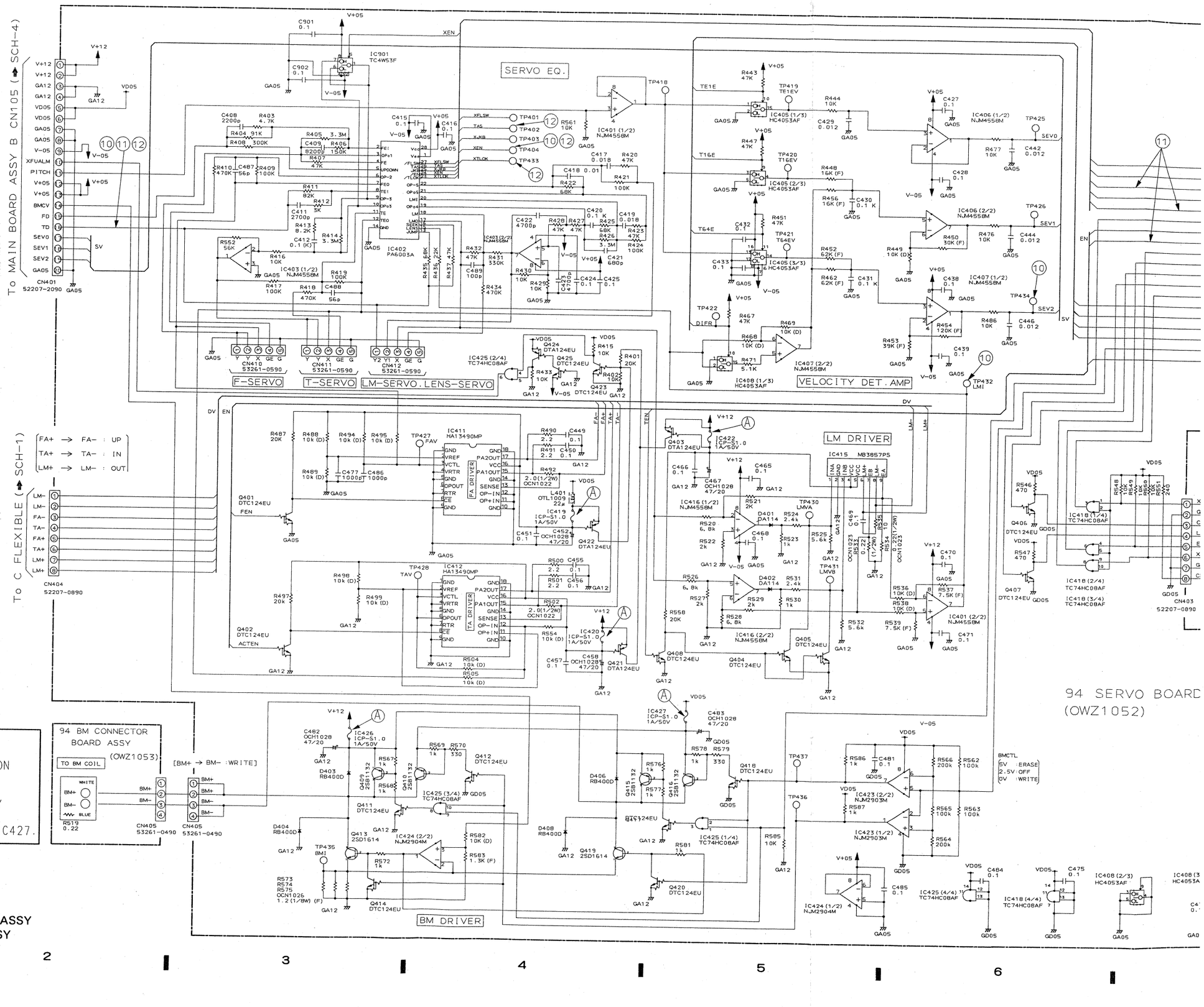
Note :*1 This product uses the not effective side for MASS format disk discrimination.


TO INTERFACE FOR THE CHANGER
CN408
CN407
94CHANGER I/F BOAD ASSY
(OWZ1054) (➡SCH-3)
XEJSW2 GD05 CLAMP LOAD ESYNC XETRK GD05 CHECK5
RS-232C
CN109
TXD RXD GND +5V
JUMPER PIN
CN301
GND SCSI ID0 GND SCSI ID1 GND SCSI ID2 GND Parity Check GND E.JSW RES GND PWON RES GND MODE 0 GND MODE 1 GND TERM
SCH-1
CN101
SCSI
GD05 XSD0 GD05 XSD1 GD05 XSD2 GD05 XSD3 GD05 XSD4 GD05 XSD5 GD05 XSD6 GD05 XSD7 GD05 XSDP GD05 GD05 GD05 GD05 GD05 GD05 NC TERMPW GD05 GD05 GD05 GD05 GD05 XSATN GD05 GD05 GD05 XSBSYO GD05 XSACKO GD05 XRSTO GD05 XSMSG GD05 XSSELO GD05 XSCD GD05 XSREQO GD05 XSIO +5V GND GND +12V
GND -DB0 GND -DB1 GND -DB2 GND -DB3 GND -DB4 GND -DB5 GND -DB6 GND -DB7 GND -DBP GND GND GND GND GND GND GND OPEN TERMPWR GND GND GND GND GND -ATN GND GND GND -BSY GND -ACK GND -RST GND -MSG GND -SEL GND -C/D GND -REQ GND -I/O
POWER
FUJI CARD ODX1004
CN403
XEJSW2 GD05 CLAMP LOAD ESYNC XETRK GD05 CHECK5
CN401
V+12 V+12 GA12 GA12 VD05 VD05 GA05 GA05 V-05 XFUALM PITCH V+05 V+05 BMCV FD TD SEV0 SEV1 SEV2 GA05
FUJI CARD ODX1003
CN105
V+12 V+12 GA12 GA12 VD05 VD05 GA05 GA05 V-05 XFUALM PITCH V+05 V+05 BMCV FD TD SEV0 SEV1 SEV2 GA05
F-SERVO
CN410
Y Y X GE G
T-SERVO
CN411
Y Y X GE G
LM-SERVO
LENSE-SERVO
CN412
Y2 Y1 X GE G
94SERVO BOARD ASSY
(OWZ1052) (➡SCH-3)
CN402
GD05 XJKB XEN XTLOK XFLSW TAS BMBST FEN TEN EXSYNC XEXTRK XCLAMP XLOAD XEJSW1 TE1E T16E T64E DIFR BMCTL ACTEN
CN107
GD05 XJKB XEN XTLOK XFLSW TAS BMBST FEN TEN EXSYNC XEXTRK XCLAMP XLOAD XEJSW1 TE1E T16E T64E DIFR BMCTL ACTEN
FUJI CARD ODX1003
MAIN BOARD ASSY B
(OEA1021)
(➡SCH-4, 5)
SERVO BOARD ASSY (OEA1019)
CN405
BM+ BM+ BM- BM-
CN404
LM- LM- FA- TA- FA+ TA+ LM+ LM+
94 BM CONNECTOR BOARD ASSY
(OWZ1053)
(➡SCH-3)
BM+ BM-
BM COIL ASSY
OTL1051
C FLEXIBLE
(ONP1089)
FA+ FA- TA+ TA- LM+ LM-
FACT TACT LM
Det.A
Det.B
PD FLEXIBLE
(ONP1077)
GA05 D1 C1 D2 C2 COMA C3 D3 COMB C4 D4 GA05
PU BOARD ASSY
(OEA1020)
(➡SCH-2)
CN102
V+10 V+05 V-05 MORF- MORF+ GA05 PPRF- GA05 FE M1RR
CN103
VD05 OSCLCT V6.2 RVC WVC CSSW GD05 WDTG SSMR GD05
FUJI CARD ODX1002
CN4
CN1
CN3
CN2
OSCLCT LD GD05 V+10 MDA GD05
940SC BOARD ASSY B
(OWX1090)
(➡SCH-2)
LD
LD FLEXIBLE 130
(ONP1078)
MD
CN108
FG SPCNT GND SPF SPP HALL VCC
SPINDLE MOTOR
(CXM1015)
CN106
EM+ EM-
CN.ASSY
ODF1008
LODING DRIVE ASSY
(OWY1051)

4.2 PU BOARD ASSY AND 94 OSC BOARD ASSY



4.3 94 SERVO BOARD ASSY, 94 BM CONNECTOR BOARD ASSY AND 94 CHANGER I/F BOARD ASSY



● CAUTION:

FOR CONTINUED PROTECTION AGAINST RISK OF FIRE. REPLACE ONLY WITH SAME TYPE NO. ICP-S1.0, MFD BY ROHM CO., LTD. FOR IC419, IC420, IC422, IC426 AND IC427.

SCH−3 94 SERVO BOARD ASSY, 94 BM CONNECTOR BOARD ASSY 94 CHANGER I/F BOARD ASSY

SCH-3

SERVO EQ.

VELOCITY DET. AMP

LM DRIVER

BM DRIVER

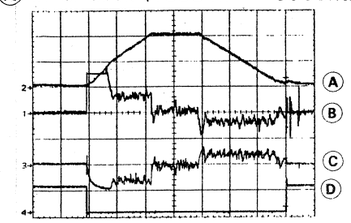
94CHANGER I/F BOAD ASSY (OWZ1054)

94 SERVO BOARD ASSY (OWZ1052)

To MAIN BOARD ASSY B CN107 (SCH-4)

To INTERFACE FOR THE CHANGER

⑩ Inner Seek (1000 htr → 3000htr) Operation*10



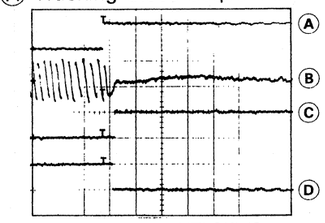
Trigger: TP404 (XEN) (94 SERVO BOARD ASSY)

Ⓐ: TP434 (SEV2) 1 V/div. DC
Ⓑ: CN401 Pin16 (TD) 1 V/div. DC
Ⓒ: TP432 (LMI) 200 V/div. DC
Ⓓ: TP404 (XEN) 5 V/div. DC
Time/div.: 10 msec./div.

*10: The following commands are transmitted from the 232C port (CN109: MAIN BOARD ASSY B), and then the seek command is put out

- Pause OFF
- Spindle ON
- LD ON
- Focus Close
- Tracking Close

⑪ Tracking Close Sequential*11

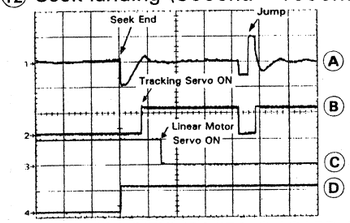


Trigger: CN402 Pin4 (XTLOK) (Strage ocsilloscope)

Ⓐ: CN402 Pin9 (TEN) 5 V/div. DC
Ⓑ: CN401 Pin16 (TD) 1 V/div. DC
Ⓒ: CN402 Pin6 (TAS) 5 V/div. DC
Ⓓ: CN402 Pin4 (XTLOK) 5 V/div. DC
Time/div.: 1 msec./div.

*11: In the same way as for ④, the waveform at the moment when tracking has been closed.

⑫ Seek landing (3000htr→1000htr) Operation*12



Trigger: TP404 (XEN) (94 SERVO BOARD ASSY)

Ⓐ: CN401 Pin16 (TD) 1 V/div. DC
Ⓑ: TP402 (TAS) 5 V/div. DC
Ⓒ: TP433 (XTLOK) 5 V/div. DC
Ⓓ: TP404 (XEN) 5 V/div. DC
Time/div.: 10 msec./div.

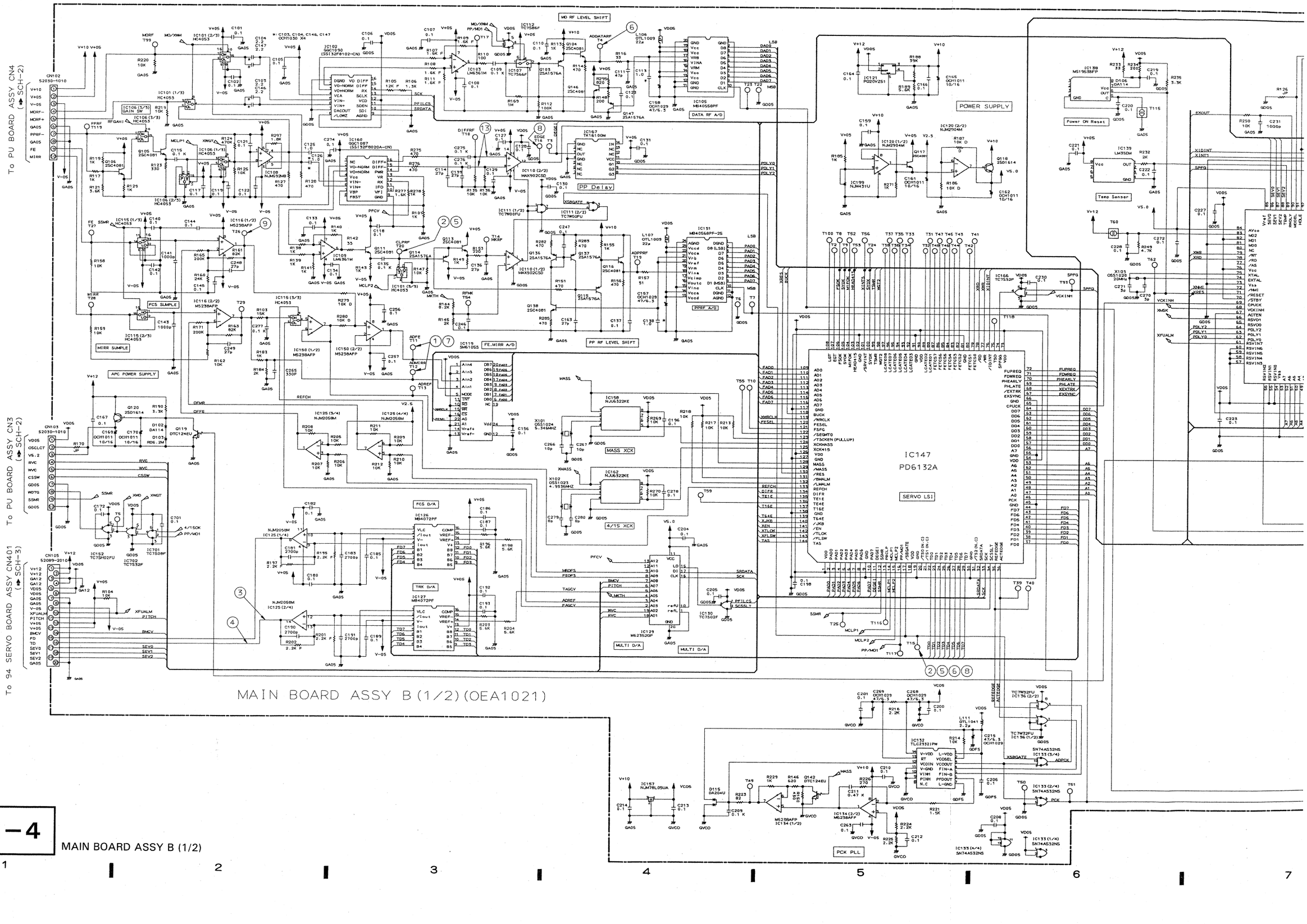
*12: The following commands are transmitted from the 232C port (CN109: MAIN BOARD ASSY B), and then the seek command is put out:

- Pause OFF
- Spindle ON
- LD ON
- Focus Close
- Tracking Close

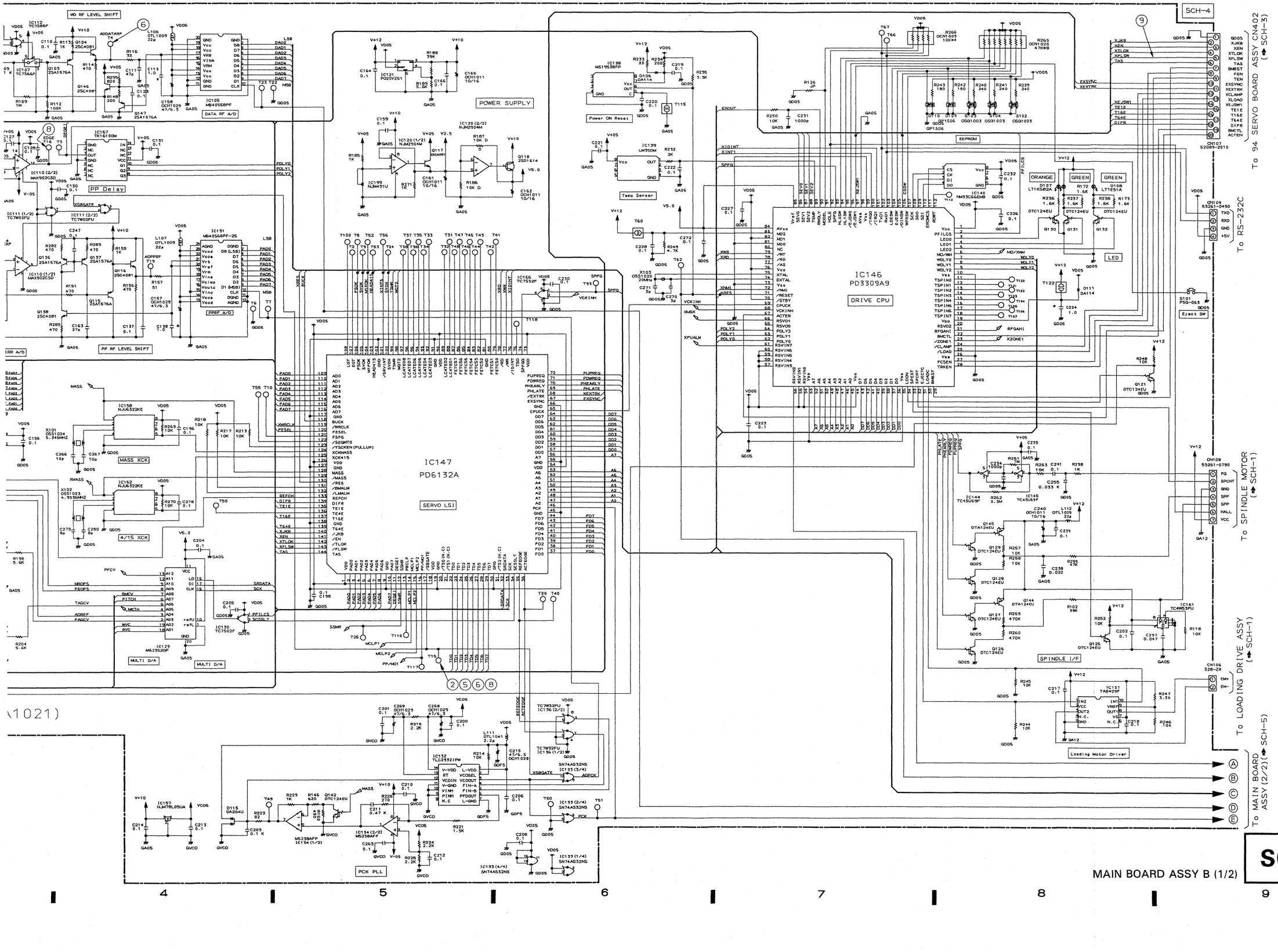
94 SERVO BOARD ASSY,
94 BM CONNECTOR BOARD ASSY
94 CHANGER I/F BOARD ASSY

SCH-3

4.4 MAIN BOARD ASSY B



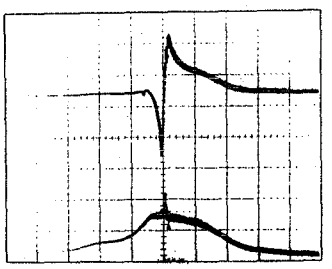
SCH-4


MO RF LEVEL SHIFT
DATA RF A/D
POWER SUPPLY
Power ON Reset
Temp Sensor
EEPROM
PP Delay
PP RF LEVEL SHIFT
PPRF A/D
IRR A/D
IC146
PD3309A9
DRIVE CPU
LED
IC147
PD6132A
SERVO LSI
MASS XCK
4/15 XCK
MULTI D/A
PCK PLL
SPINDLE I/F
Loading Motor Driver
SCH-4
To 94 SERVO BOARD ASSY CN402 (◆SCH-3)
To RS-232C
To SPINDLE MOTOR (◆SCH-1)
To LOADING DRIVE ASSY (◆SCH-1)
To MAIN BOARD ASSY (2/2)(◆SCH-5)
MAIN BOARD ASSY B (1/2)
SCH-4

● Waveforms

Note: This is the waveform with use of a MASS format disc (DEC−17GMO, DC−17GWO).

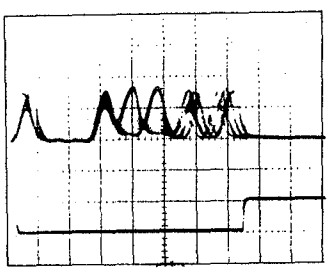
① Focus Up/Down Operation *1



Trigger: TP11 (ADFE)
Upper: TP11 (ADFE) 500 mV/div. DC
Lower: TP12 (ADMIRR) 1 V/div. DC
Time/div.: 5 msec./div.

*1: The following commands are transmitted from the 232C port (CN109: MAIN BOARD ASSY B):
- Pause OFF
- Spindle ON
- LD ON
- Focus Up/Down

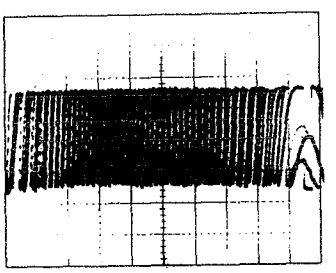
② Focus Close (Tracking Open)State *2



Trigger: TP15 (XSBGATE)
Upper: TP20 (CLPRF) 1 V/div. DC
Lower: TP15 (XSBGATE) 5 V/div. DC.
Time/div.: 0.2 μsec./div.

*2: The following commands are transmitted from the 232C port (CN109: MAIN BOARD ASSY B):
- Pause OFF
- Spindle ON
- LD ON
- Focus Close

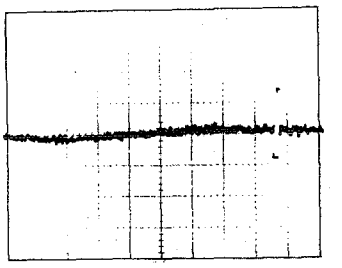
③ Focus Close (Tracking Open) State *3



Trigger: TP55 (XSEGMT0)
CN105 Pin16 (TD): 500 mV/div. DC
Time/div.: 1 msec./div.

*3: The following commands are transmitted from the 232C port (CN109: MAIN BOARD ASSY B):
- Pause OFF
- Spindle ON
- LD ON
- Focus Close

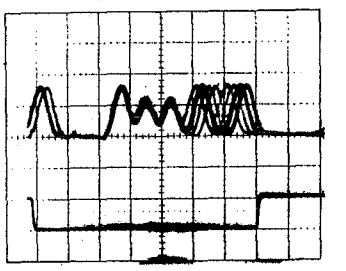
④ Tracking Close (Pause) State *4



Trigger: TP55 (XSEGMT0)
CN105 Pin16 (TD): 500 mV/div. DC
Time/div.: 2 msec./div.

*4: The following commands are transmitted from the 232C port (CN109: MAIN BOARD ASSY B):
- Pause OFF
- Spindle ON
- LD ON
- Focus Close
- Tracking Close

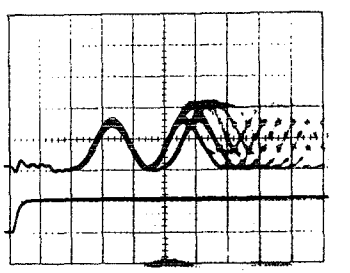
⑤ Tracking Close State*5



Trigger: TP15 (XSBGATE)
Upper: TP20 (CLPRF) 1 V/div. DC
Lower: TP15 (XSBGATE) 5 V/div. DC
Time/div.: 0.2 μsec./div.

*5: The following commands are transmitted from the 232C port (CN109: MAIN BOARD ASSY B):
- Pause OFF
- Spindle ON
- LD ON
- Focus Close
- Tracking Close

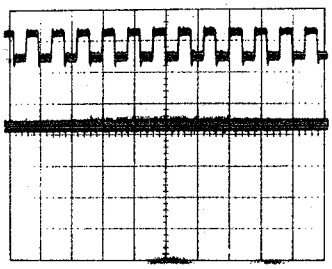
⑥ Tracking Close State*6 (DATA section、 when Read)



Trigger: TP15 (XSBGATE)
Upper: TP4 (ADDATARF) 500 mV/div. AC
Lower: TP15 (XSBGATE) 5 V/div. DC
Time/div.: 50 nsec./div.

*6: The following commands are transmitted from the 232C port (CN109: MAIN BOARD ASSY B), and then seeking is done for the track where the data are written.
- Pause OFF
- Spindle ON
- LD ON
- Focus Close
- Tracking Close

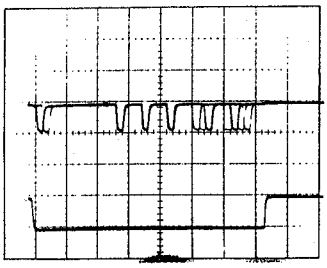
⑦ Focus Close State *7



Trigger: TP11 (ADFE)
Upper: TP11 (ADFE) 500 mV/div. DC
Lower: TP12 (ADMIRR) 500 mV/div. DC.
Time/div.: 5 μsec./div.

*7: The following commands are transmitted from the 232C port (CN109: MAIN BOARD ASSY B):
- Pause OFF
- Spindle ON
- LD ON
- Focus Close

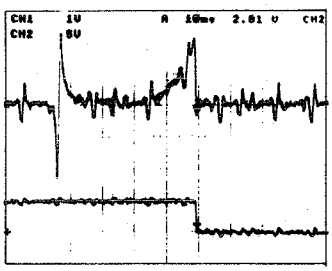
⑧ Edge Waveform (Tracking Close) State *8



Trigger: TP15 (XSBGATE)
Upper: TP16 (EDGE) 5 V/div. DC
Lower: TP15 (XSBGATE) 5 V/div. DC
Time/div.: 0.2 μsec./div.

*8: The following commands are transmitted from the 232C port (CN109: MAIN BOARD ASSY B):
- Pause OFF
- Spindle ON
- LD ON
- Focus Close
- Tracking Close

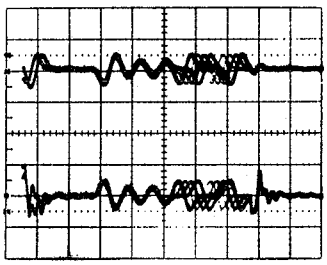
⑨ Focus Close Sequential*9



Trigger: CN107 Pin5 (XFLSW) (strage oscilloscope)
Upper: TP26 (FE) 1 V/div. DC
Lower: CN107 Pin5 (XFLSW) 5 V/div. DC.
Time/div.: 10 msec./div.

*9: The following commands are transmitted from the 232C port (CN109: MAIN BOARD ASSY B):
- Pause OFF
- Spindle ON
- LD ON
- Focus Close

⑬ Differential Waveform (Tracking Close) State*13



Trigger: TP15 (XSBGATE)
Upper: IC110 Pin9 1 V/div. DC
Lower: IC110 Pin8 1 V/div. DC.
Time/div.: 0.2 μsec./div.

*13: Transmission from the 232C port (CN109: MAIN BOARD ASSY B):
- Pause OFF (Enter Test Mode)
  The following command is transmitted from the SCSI port (CN101: MAIN BOARD ASSY B), and then seeking is done for any address.
- Start up

MAIN BOARD ASSY B (2/2) (OEA1021)

IC319
PD6056A
4/15 MSC

IC311
M8441-55PFQ
SRAM

IC310
PD6077
4/15 ECC

IC328
PD6133A
Read/Write LSI

IC338 GQC1099 (MB814400A-70P-JN) DRAM

IC339 GQC1099 (MB814400A-70P-JN) DRAM

IC333 OYW1076 (M28F020-120) FROM

IC334 LC35064M-80 PSRAM

Controller ROM

WRITE DELAY

IC128 TK15100M

IC342 (2/3) SN74ALS11ANS

IC135 TC7SH08FU

IC135 (1/2) TC7W32FU

IC135 (2/2) TC7W32FU

IC345 (4/8) IC345 (3/8) IC345 (2/8) TC74HC254AF

IC345 (1/8) IC345 (6/8) IC345 (7/8) IC345 (5/8) TC74HC245AF

IC346 TLC29321PW

IC324 TLC29321PW

IC326 (1/2) M6238AFP

IC326 (2/2) M6238AFP

IC352 (1/2) TC7W02FU

IC352 (2/2) TC7W02FU

IC348 NJM78L05UA

IC301 GQC1013 (SMC) 50MHz

IC309 PD6076

L301 DTL1041 2.2μH

L338 DCHT029 470/6.3

T301 T302 T303 T304 T305 T306 T307 T308 T309 T310 T311 T312 T313 T314 T315 T316 T317 T318 T319 T320 T321 T322 T323 T324 T325 T326 T327 T328 T329 T330 T331 T332 T333 T334 T335 T336 T337 T338 T339 T340 T341 T342 T343 T344 T345 T346 T347 T348 T349 T350 T351 T352

Q305 DTA124EU

Q306 DTC124EU

Q309 DTC124EU

Q310 DTA124EU

Q301 DTC124EU

Q302 DTA124EU

Q303 DTA114EU

Q304 DA114

Q505 DTC124EU

D305 DA204U

D304 DA114

R331 QCX1007 10KX8

R333 QCX1007-A 10KX8

R302 QCX1007 10KX8

R313 3K

R316 10K

R318 1.8K F

R319 2.2K

R321 2.2K

R322 2.2K

R328 82

R329 1K

R336 1.8K F

R337 360

R338 240

R344 10K

R352 0.1 K

R505 0.47 K

R320 470

C306 0.1

C309 0.1

C310 0.1

C311 0.1

C315 0.1

C319 0.1

C320 0.1

C325 0.1

C326 (1/2) M6238AFP

C327 0.1

C329 0.1

C330 0.47 K

C331 0.1

C334 0.1

C335 0.1

C336 0.1

C339 0.1

C345 0.1

C346 0.1

C347 0.1

C348 0.1

C351 0.1

C352 0.1 K

C354 0.1

C355 0.1

C356 0.1

C357 0.1

C360 0.1

C362 0.1

C374 DCHT029 470/6.3

C376 0.1

C377 0.1

C378 0.1

C380 0.1

C377 DCHT029 470/6.3

C203 0.1

C140 0.1

C344 0.1

V405

V-05

V+10

V+12

VDD5

VDF5

GVCO

GDF5

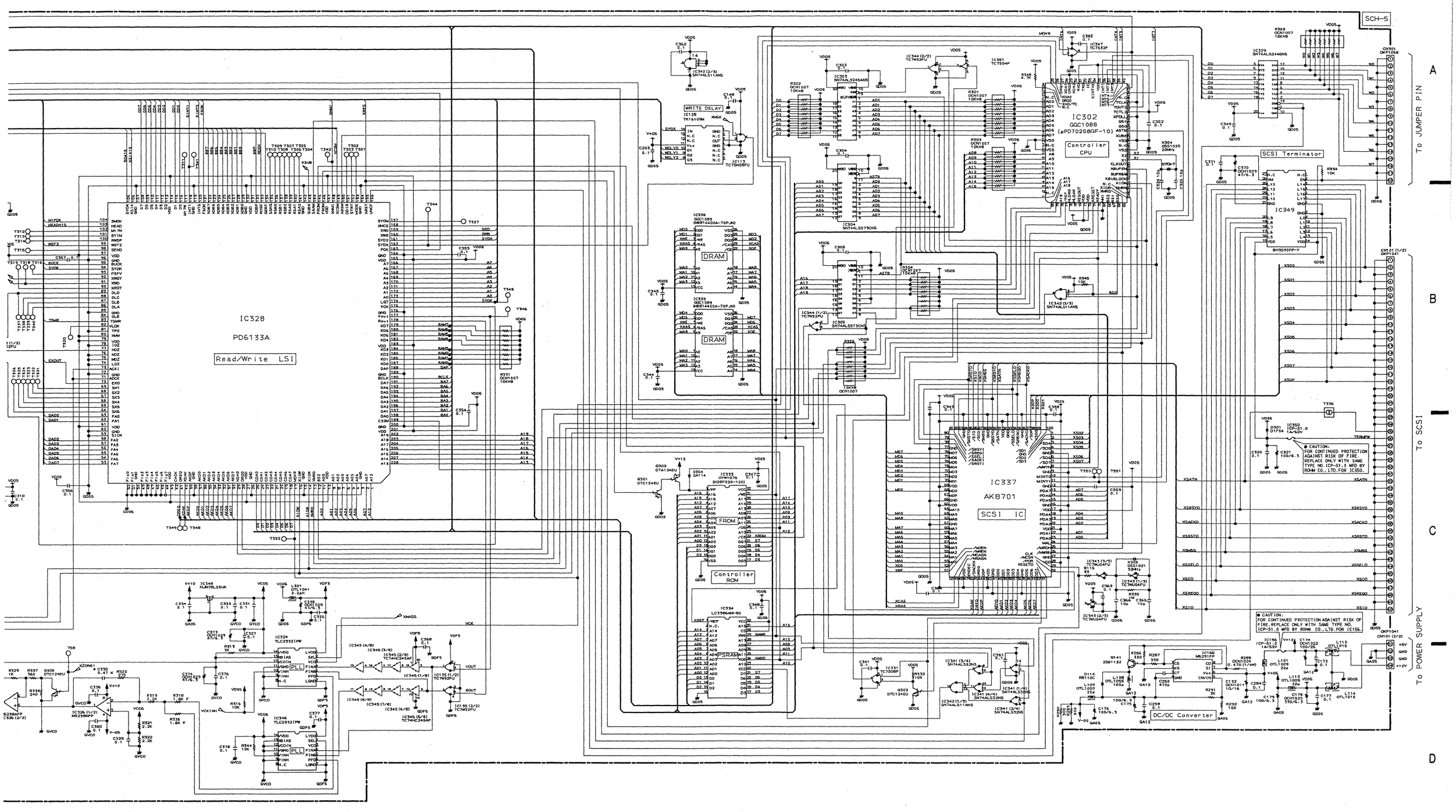
GD05

VCK PLL

To MAIN BOARD ASSY B(1/2) (→ SCH-4)

SCH-5

MAIN BOARD ASSY B (2/2)



MAIN BOARD ASSY B (2/2)

SCH-5

5. PCB PARTS LIST

NOTES :

- *Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*
- *When ordering resistors, first convert resistance values into code form as shown in the following examples.*

Ex. 1 When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J = 5%, and K = 10%).

560Ω → 56 × 10¹ → 561 ····· RD1/8PM [5][6][1] J
47kΩ → 47 × 10³ → 473 ····· RD1/4PS [4][7][3] J
0.5Ω → 0R5 ····· RN2H [0][R][5] K
1Ω → 010 ····· RS1P [0][1][0] K

Ex. 2 When there are 3 effective digits (such as in high precision metal film resistors).

5.62kΩ → 562 × 10¹ → 5621 ····· RM1/4PC [5][6][2][1] F

Mark	No.	Description	Parts No.
LIST OF ASSEMBLIES			
		MAIN BOARD ASSY B	OEA1021
		SERVO BOARD ASSY	OEA1019
NSP		├─94 SERVO BOARD ASSY	OWZ1052
NSP		├─94 BM CONNECTOR BOARD ASSY	OWZ1053
NSP		└─94 CHANGER I/F BOARD ASSY	OWZ1054
		PU BOARD ASSY	OEA1020
NSP		94 OSC BOARD ASSY	OWX1090
MAIN BOARD ASSY B			
SEMICONDUCTORS			
	IC337		AK8701
	IC349		BH9590FP−Y
	IC156, IC350		ICP−S1.0
	IC334		LC33864M−80
	IC139		LM35DM
	IC103, IC109		LM6361M
	IC138		M51953BFP
	IC116, IC134, IC150, IC326		M5238AFP
	IC155		M5291FP
	IC129		M62352GP
	IC110		MAX902CSD
	IC105		MB40558PF
	IC151		MB40568PF−25
	IC126, IC127		MB4072PF
	IC338, IC339 (MB814400A−70PJN)		GGC1089
	IC311		MB8441−55PFQ
	IC125		NJM2058M
	IC120		NJM2904M
	IC199		NJM431U
	IC108		NJM592M8
	IC157, IC348		NJM78L05UA
	IC158, IC162		NJU6322KE
	IC140		NM93C66EM8
	IC146		PD3309A9
	IC319		PD6056A
	IC309		PD6076
	IC310		PD6077
	IC147		PD6132A
	IC328		PD6133A
	IC121		PQ20VZ51
	IC333 CONTROLLER ROM		OWY1076
	IC119		SM6105S
	IC342		SN74ALS11ANS
	IC329		SN74ALS244BNS
	IC303		SN74ALS245ANS
	IC341		SN74ALS32NS
	IC304, IC305		SN74ALS573CNS
	IC133		SN74AS32NS
	IC160 (SSI32F8020A−CN)		GGC1087
	IC102 (SSI32F8102−CN)		GGC1090
	IC137		TA8409F
	IC144, IC145		TC4SU69F
	IC161		TC4W53FU
	IC345		TC74HC245AF
	IC101, IC106, IC115		TC74HC4053AF
	IC130		TC7S02F
	IC351		TC7S04F
	IC331, IC701		TC7S08F
	IC166, IC347, IC702		TC7S32F
	IC107		TC7S66F
	IC112		TC7S86F
	IC152		TC7SH02FU
	IC113		TC7SH08FU
	IC111		TC7W00FU
	IC352		TC7W02FU
	IC135, IC136, IC344		TC7W32FU
	IC343		TC7WU04FU
	IC128, IC167		TK16100M
	IC132, IC324, IC346		TLC2932IPW
	IC302 (UPD70208GF−10−3B9)		GGC1088
	Q103, Q114, Q115, Q136, Q137		2SA1576A
	Q147		2SA1576A
	Q141		2SB1132
	Q104−Q106, Q111, Q113		2SC4081
	Q116, Q117, Q138, Q146		2SC4081
	Q118, Q120		2SD1614
	Q144, Q145, Q302		DTA124EU
	Q119, Q121, Q125−Q132, Q142		DTC124EU
	Q301, Q303, Q305		DTC124EU
	D301		D1FS4
	D102, D106, D111, D304		DA114
	D115, D305		DA204U
	D109, D110		GP1S06
	D108		LT1E51A
	D107		LT1KS82A
	D114		RB110C
	D103		RD6.2MB1/B2
COILS AND FILTERS			
	L101, L106, L107, L109, L110 (22μH)		OTL1009
	L112 (22μH)		OTL1009
	L113, L114		OTL1015
	L111, L301 (2.2μH)		OTL1041
	L108 (100μH)		OTL1055
SWITCHES AND RELAYS			
	S102−S104		OSG1003
	S101		PSG−063
CAPACITORS			
	C270, C271		CCSQCH030C50
	C266, C267, C279, C280		CCSQCH080D50
	C324, C325, C365, C366		CCSQCH100D50
	C114, C136, C139, C163		CCSQCH270J50
	C248, C249		CCSQCH270J50
	C265		CCSQCH331J50
	C111		CCSQCH470J50
	C250		CCSQCH471J50
	C141, C143, C231, C234		CCSQSL102J50
	C175, C176, C179, C321		CEV101M6R3
	C109, C115, C135, C209, C241		CKSQYB104K25
	C275−C277, C332		CKSQYB104K25
	C238		CKSQYB223K50
	C181, C183, C190, C191		CKSQYB272K50
	C255		CKSQYB333K25
	C237		CKSQYB473K50
	C101, C102, C105−C108, C110		CKSQYF104Z50
	C117−C119, C121−C123		CKSQYF104Z50
	C127−C131, C133, C134, C137		CKSQYF104Z50
	C140, C142, C144, C145, C148		CKSQYF104Z50
	C156, C159, C164, C166, C167		CKSQYF104Z50
	C172, C173, C177, C180, C182		CKSQYF104Z50
	C185−C187, C189, C192, C193		CKSQYF104Z50
	C196, C198, C200−C206, C208		CKSQYF104Z50
	C210, C212−C214, C217−C223		CKSQYF104Z50
	C226−C228, C230, C232, C235		CKSQYF104Z50
	C239, C246, C247, C256−C258		CKSQYF104Z50
	C263, C272, C274, C278, C284		CKSQYF104Z50
	C302−C306, C309−C311		CKSQYF104Z50
	C319, C320, C326, C327, C329		CKSQYF104Z50
	C331, C333, C334, C336, C341		CKSQYF104Z50
	C343−C345, C347−C349, C351		CKSQYF104Z50
	C353, C354, C356−C362		CKSQYF104Z50
	C368, C369, C371, C376−C378		CKSQYF104Z50
	C380, C382, C701		CKSQYF104Z50
	C113, C125, C126, C138, C224		CKSYF105Z16
	C132, C161, C162, C165 (10μF/16V)		OCH1011
	C169, C170, C240 (10μF/16V)		OCH1011
	C174 (100μF/25V)		OCH1022
	C178 (330μF/6.3V)		OCH1025
	C157, C158, C215, C268, C269 (47μF/6.3V)		OCH1029
	C335, C370, C373, C374 (47μF/6.3V)		OCH1029
	C103, C104, C146, C147 (2.2μF/16V)		OCH1030
	C211, C330 (0.47μF/16V)		OCH1031
	C160		CCSSL222J50
RESISTORS			
	R301−R305, R308, R331, R333 (10KΩ×8)		OCN1007
	R266 (10KΩ×4)		OCN1009
	R265 (47KΩ×8)		OCN1020
	R288 (0.47Ω, 1/4W)		OCN1024
	R186, R187, R279, R280		RN1/10SE103D
	R105		RS1/10S123F
	R107−R109, R111		RS1/10S162F
	R318, R336		RS1/10S182F
	R195, R197, R201, R202		RS1/10S222F
	Other Resistors		RS1/10S□□□J
OTHERS			
	CN102, CN103 CONNECTOR		52030−1010
	CN105, CN107 CONNECTOR		52089−2010
	CN109 CONNECTOR		53261−0490
	CN108 CONNECTOR		53261−0790
	CN101 SCSI CONNECTOR		OKP1041
	CN301 CONNECTOR (18P)		OKP1058
	X301 (50MHz)		OSS1013
	X103, X304 (20MHz)		OSS1020
	X305 (32MHz)		OSS1021
	X102 (4.9536MHz)		OSS1023
	X101 (5.346MHz)		OSS1024
	IC333 (IC SOCKET)		OKH1019
94 SERVO BOARD ASSY			
SEMICONDUCTORS			
	IC411, IC412		HA13490MP
	IC419, IC420, IC422, IC426, IC427		ICP−S1.0
	IC415		MB3857PS
	IC423		NJM2903M
	IC424		NJM2904M
	IC401, IC403, IC406, IC407, IC416		NJM4558M
	IC402		PA6003A
	IC901		TC4W53F
	IC418, IC425		TC74HC08AF
	IC405, IC408		TC74HC4053AF
	Q409, Q410, Q415, Q416		2SB1132
	Q413, Q419		2SD1614
	Q403, Q421, Q422, Q424		DTA124EU
	Q401, Q402, Q404−Q408		DTC124EU
	Q411, Q412, Q414, Q417, Q418		DTC124EU
	Q420, Q423, Q425		DTC124EU
	D401, D402		DA114
	D403, D404, D406, D408		RB400D
COILS AND FILTERS			
	L401 (22μH)		OTL1009
CAPACITORS			
	C489		CCSQCH101J50
	C487, C488		CCSQCH560J50
	C477, C486		CCSQSL102J50
	C421		CCSQSL681J50
	C418		CKSQYB103K50
	C412, C420, C430, C431		CKSQYB104K25
	C429, C442, C444, C446, C422		CKSQYB123K50
	C417, C419		CKSQYB183K50
	C408		CKSQYB222K50
	C411		CKSQYB272K50
	C423		CKSQYB562K50
	C409		CKSQYB822K50
	C415, C416, C424, C425		CKSQYF104Z50
	C427, C428, C432, C433		CKSQYF104Z50
	C438, C439, C449−C451		CKSQYF104Z50

Mark	No.	Description	Parts No.
	D107		LT1KS82A
	D114		RB110C
	D103		RD6.2MB1/B2
COILS AND FILTERS			
	L101, L106, L107, L109, L110	(22μH)	OTL1009
	L112	(22μH)	OTL1009
	L113, L114		OTL1015
	L111, L301	(2.2μH)	OTL1041
	L108	(100μH)	OTL1055
SWITCHES AND RELAYS			
	S102−S104		OSG1003
	S101		PSG−063
CAPACITORS			
	C270, C271		CCSQCH030C50
	C266, C267, C279, C280		CCSQCH080D50
	C324, C325, C365, C366		CCSQCH100D50
	C114, C136, C139, C163		CCSQCH270J50
	C248, C249		CCSQCH270J50
	C265		CCSQCH331J50
	C111		CCSQCH470J50
	C250		CCSQCH471J50
	C141, C143, C231, C234		CCSQSL102J50
	C175, C176, C179, C321		CEV101M6R3
	C109, C115, C135, C209, C241		CKSQYB104K25
	C275−C277, C332		CKSQYB104K25
	C238		CKSQYB223K50
	C181, C183, C190, C191		CKSQYB272K50
	C255		CKSQYB333K25
	C237		CKSQYB473K50
	C101, C102, C105−C108, C110		CKSQYF104Z50
	C117−C119, C121−C123		CKSQYF104Z50
	C127−C131, C133, C134, C137		CKSQYF104Z50
	C140, C142, C144, C145, C148		CKSQYF104Z50
	C156, C159, C164, C166, C167		CKSQYF104Z50
	C172, C173, C177, C180, C182		CKSQYF104Z50
	C185−C187, C189, C192, C193		CKSQYF104Z50
	C196, C198, C200−C206, C208		CKSQYF104Z50
	C210, C212−C214, C217−C223		CKSQYF104Z50
	C226−C228, C230, C232, C235		CKSQYF104Z50
	C239, C246, C247, C256−C258		CKSQYF104Z50
	C263, C272, C274, C278, C284		CKSQYF104Z50
	C302−C306, C309−C311		CKSQYF104Z50
	C319, C320, C326, C327, C329		CKSQYF104Z50
	C331, C333, C334, C336, C341		CKSQYF104Z50
	C343−C345, C347−C349, C351		CKSQYF104Z50
	C353, C354, C356−C362		CKSQYF104Z50
	C368, C369, C371, C376−C378		CKSQYF104Z50
	C380, C382, C701		CKSQYF104Z50
	C113, C125, C126, C138, C224		CKSYF105Z16
	C132, C161, C162, C165	(10μF/16V)	OCH1011
	C169, C170, C240	(10μF/16V)	OCH1011
	C174	(100μF/25V)	OCH1022
	C178	(330μF/6.3V)	OCH1025
	C157, C158, C215, C268, C269	(47μF/6.3V)	OCH1029
	C335, C370, C373, C374	(47μF/6.3V)	OCH1029
	C103, C104, C146, C147	(2.2μF/16V)	OCH1030
	C211, C330	(0.47μF/16V)	OCH1031
	C160		CCSSL222J50
RESISTORS			
	R301−R305, R308, R331, R333 (10KΩ×8)		OCN1007
	R266	(10KΩ×4)	OCN1009

Mark	No.	Description	Parts No.
	R265	(47KΩ×8)	OCN1020
	R288	(0.47Ω, 1/4W)	OCN1024
	R186, R187, R279, R280		RN1/10SE103D
	R105		RS1/10S123F
	R107−R109, R111		RS1/10S162F
	R318, R336		RS1/10S182F
	R195, R197, R201, R202		RS1/10S222F
	Other Resistors		RS1/10S□□□J
OTHERS			
	CN102, CN103	CONNECTOR	52030−1010
	CN105, CN107	CONNECTOR	52089−2010
	CN109	CONNECTOR	53261−0490
	CN108	CONNECTOR	53261−0790
	CN101	SCSI CONNECTOR	OKP1041
	CN301	CONNECTOR (18P)	OKP1058
	X301	(50MHz)	OSS1013
	X103, X304	(20MHz)	OSS1020
	X305	(32MHz)	OSS1021
	X102	(4.9536MHz)	OSS1023
	X101	(5.346MHz)	OSS1024
	IC333 (IC SOCKET)		OKH1019
94 SERVO BOARD ASSY			
SEMICONDUCTORS			
	IC411, IC412		HA13490MP
	IC419, IC420, IC422, IC426, IC427		ICP−S1.0
	IC415		MB3857PS
	IC423		NJM2903M
	IC424		NJM2904M
	IC401, IC403, IC406, IC407, IC416		NJM4558M
	IC402		PA6003A
	IC901		TC4W53F
	IC418, IC425		TC74HC08AF
	IC405, IC408		TC74HC4053AF
	Q409, Q410, Q415, Q416		2SB1132
	Q413, Q419		2SD1614
	Q403, Q421, Q422, Q424		DTA124EU
	Q401, Q402, Q404−Q408		DTC124EU
	Q411, Q412, Q414, Q417, Q418		DTC124EU
	Q420, Q423, Q425		DTC124EU
	D401, D402		DA114
	D403, D404, D406, D408		RB400D
COILS AND FILTERS			
	L401	(22μH)	OTL1009
CAPACITORS			
	C489		CCSQCH101J50
	C487, C488		CCSQCH560J50
	C477, C486		CCSQSL102J50
	C421		CCSQSL681J50
	C418		CKSQYB103K50
	C412, C420, C430, C431		CKSQYB104K25
	C429, C442, C444, C446, C422		CKSQYB123K50
	C417, C419		CKSQYB183K50
	C408		CKSQYB222K50
	C411		CKSQYB272K50
	C423		CKSQYB562K50
	C409		CKSQYB822K50
	C415, C416, C424, C425		CKSQYF104Z50
	C427, C428, C432, C433		CKSQYF104Z50
	C438, C439, C449−C451		CKSQYF104Z50

Mark	No.	Description	Parts No.
	C455−C457, C465, C466		CKSQYF104Z50
	C468−C471, C475, C478, C479		CKSQYF104Z50
	C481, C484, C485, C901, C902		CKSQYF104Z50
	C452, C458, C467, C482, C483	(47μF/20V)	OCH1028
RESISTORS			
	R492, R502	(2Ω, 1/2W)	OCN1022
	R533, R534	(0.22Ω, 1/2W)	OCN1023
	R573−R575	(1.2Ω, 1/8W)	OCN1026
	R444, R449, R468, R469		RN1/10SE103D
	R488, R489, R494, R495		RN1/10SE103D
	R498, R499, R504, R505, R536		RN1/10SE103D
	R538, R554, R582		RN1/10SE103D
	R454		RS1/10S124F
	R583		RS1/10S132F
	R448, R456		RS1/10S163F
	R450		RS1/10S303F
	R453		RS1/10S393F
	R452, R462		RS1/10S623F
	R537, R539		RS1/10S752F
	Other Resistors		RS1/10S□□□J
OTHERS			
	CN405	CONNECTOR	53261−0490
	CN410−CN412	CONNECTOR	53261−0590
94 BM CONNECTOR BOARD ASSY			
RESISTORS			
	R519		RS1PMFR22J
OTHERS			
	BM JUNCTION CONNECTOR ASSY		ODF1057
94 CHANGER I/F BOARD ASSY			
OTHERS			
	CN408		OKP1055
PU BOARD ASSY			
SEMICONDUCTORS			
	IC3		AD826AR
	IC5		M5238AFP
	IC9		NJM2904M
	IC8		TC74HC123AF
	IC2		TC74HCU04AF
	IC10, IC7		TC7S32F
	IC6		TC7S66F
	IC1		UPC1663G
	Q25−Q28		2SA1424
	Q15−Q22, Q29		2SA1576A
	Q10, Q11		2SA1610
	Q23, Q24, Q3, Q6, Q9		2SC4081
	Q1, Q2, Q4, Q5		2SC4187
	Q7, Q8		2SC4187
	Q12−Q14		2SC4226
	D1, D2		GP1S560
COILS AND FILTERS			
	L1−L3	(22μH)	OTL1009
	L4	(0.56μH)	OTL1052
CAPACITORS			
	C16, C17, C41		CEV101M6R3
	C15, C43		CEV470M16
	C31, C32		CKSQYB102K50

Mark	No.	Description	Parts No.
	C29		CKSQYB103K50
	C13		CKSQYB473K50
	C1, C11, C12, C14, C18		CKSQYF104Z50
	C2, C23−C25, C27, C28		CKSQYF104Z50
	C30, C33−C36, C38−C40		CKSQYF104Z50
	C42, C44, C7−C9		CKSQYF104Z50
	C37		CKSQYF474Z16
	C3, C4, C45−C47	(0.47μF/16V)	OCH1031
	C5, C6	(0.47μF/16V)	OCH1031
RESISTORS			
	VR2	(1KΩ)	OCP1012
	VR1	(2KΩ)	OCP1021
	VR3	(200Ω)	OCP1022
	R35−R37		RN1/10SE103D
	R32, R39, R40		RS1/10S272F
	R41, R43−R48, R50		RS1/10S562F
	R1, R11, R7		RS1/10S822F
	Other Resistors		RS1/10S□□□J
94 OSC BOARD ASSY			
SEMICONDUCTORS			
	Q801, Q802		2SC4226
COILS AND FILTERS			
	L802, L803		OTL1046
	L801	(33nH)	OTL1054
CAPACITORS			
	C805		CCSRCH150J50
	C804		CCSRCH391J50
	C802		CCSRUJ101J50
	C803		CCSRUJ120J50
	C801		CCSRUJ270J50
	C806, C807		CKSRYB682K50
RESISTORS			
	R807		RS1/16S101J
	R803		RS1/16S102J
	R801, R805		RS1/16S202J
	R804		RS1/16S302J
	R802		RS1/16S752J
	Other Resistors		RS1/10S□□□J

6. TEST PROGRAM PROCEDURES

*<**CAUTION**>*
With an optical disk cartridge which can be used with the DE−UH9101.
DEC−17GMO (1.7 GB rewritable type)
DC−17GWO (1.7 GB WORM type)
DEC−702 (654 MB rewritable type)
DC−502A (654 MB WORM type)

Other optical disk cartridges can not be used, but if a wrong cartridge has been inserted by mistake, the LED will continue to flash (same as when there is no disk).
In this case, press the EJECT button and remove the optical disk cartridge.

Use the IBM PC−AT host computer and GGF1062 test program for testing. This test program can be used with the DD−5001 Series, DD−5101 Series, DE−7001 Series, DE−7101 Series, DE−UH2200 Series and DE−UH9101 Series.
With the DE−UH9101 series, inspection in rewritable mode and in WORM mode is excuted by product dip switch switching.
Use an optical disk for the Write Test (No format utility program is required to use the disk).

6.1 OVERVIEW

The test consists of four steps. Step 1 performs the controller diagnostics, Step 2 confirms the media condition, Step 3 issues commands and performs media initialization, and Step 4 performs the Aging Test.
Aging is a normal Seek Test (only the READ command does not perform error correction), and a Write/Read Test can be performed as an option. The three types of aging are as follows:

[Butterfly] : Optical head accesses while alternating between the inner tracks and outer tracks and proceeds toward the tracks.
[Random] : Optical head accesses tracks randomly.
[Constant] : Optical head accesses alternating between two specified tracks zone only.

6.2 ITEMS REQUIRED FOR TESTING

The following items are required for testing:

1) IBM PC−AT system
2) DDI−80AT interface board
3) Power cord and SCSI cable
4) System software with test software included
5) Optical disk for testing

1.Test Software

Register ANSI.SYS as the device in the CONFIG.SYS statement.

● Printer output

Test software example: ↵ : ENTER Key

B: ＼ > dir ↵

```
COMMAND  COM    24931  88-07-13   0:00
CONFIG   SYS       21  90-03-08  10:08
PRINT    SYS     5855  88-07-13   0:00
SVC      EXE    74222  90-03-08   1:00
SVC      CTL      184  90-03-08   1:00
```

● Changing the initialization values of the control file

Use the following procedure to call the file.

```
B > EDLIN _ SVC.CTL ↵
* L ↵
 1 : == Control File of SVC.EXE ==
 2 : Host ID (0-7)
 3 : 7 ..... ①
 4 : Target ID (0-7)
 5 : 0 ..... ②
 6 : LUN (0-3)
 7 : 0 ..... ③
 8 : NOB (1-80(HEX))
 9 : 80 ..... ④
10 : Output File Name (0:" SVCE.LOG ",
                       1:" (Start Time).LOG ")
11 : 0 ..... ⑤
```

① : Sets host SCSI ID=7
② : Sets target SCSI ID=0
③ : Sets LUN (Logical Unit Number)=0
④ : Sets NOB (Number Of Blocks)=80 (Hex) for number of blocks to be read. (This value is valid when Butterfly and Constant Aging.)
⑤ : Selects of filename for output of test results 0="SVCE.LOG" (fixed filename) 1=".LOG" (.LOG appended to test start time)

Example:

"03081008. LOG"····· March 8, 10:08 AM

Perform as follows to make changes:

Example:

Set Target ID to "5".
(1) *5 ↵ ····· Change 5th line of file
(2) 5: *5 ↵ ····· Target ID set to 5
(3) *E ↵ ····· Quit Editor program

2. Optical Disk for Testing

Prepare an optical disk to perform the Write Test.

6.3 TEST ITEMS

The test is performed according to the following steps.

Step 1. Controller Diagnostics

- Issues INQUIRY command
- Performs self-diagnostics using SEND DIAGNOSTIC command

Step 2. Media Condition

- Issues TEST UNIT READY command
- Issues READ CAPACITY command (data check not performed)
- Issues MODE SENSE command (checks cartridge write protected or not)

Step 3. Media Initialization

- Initializes MODE SELECT parameter
- Issues START/STOP UNIT command to spin up the bisk (for only Seek Test)
- Issues FORMAT UNIT command and clear of alternate data (for only Rewritable Write and Read Test)
- Issues VERIFY command to find an empty area for Write Test (for only WORM Write and Read Test)

Step 4. Aging Test

Menu 1: Seek Test [Butterfly]

Reads the specified number of blocks alternating between the inner tracks and outer tracks and proceeds toward the mid-tracks with the READ (Extended, ECC OFF) command. When the optical head reaches to mid-tracks, access is performed again beginning from the inner tracks and outer tracks (see Figure 1). Data checking and error correction are not performed, only the Seek Test is performed.

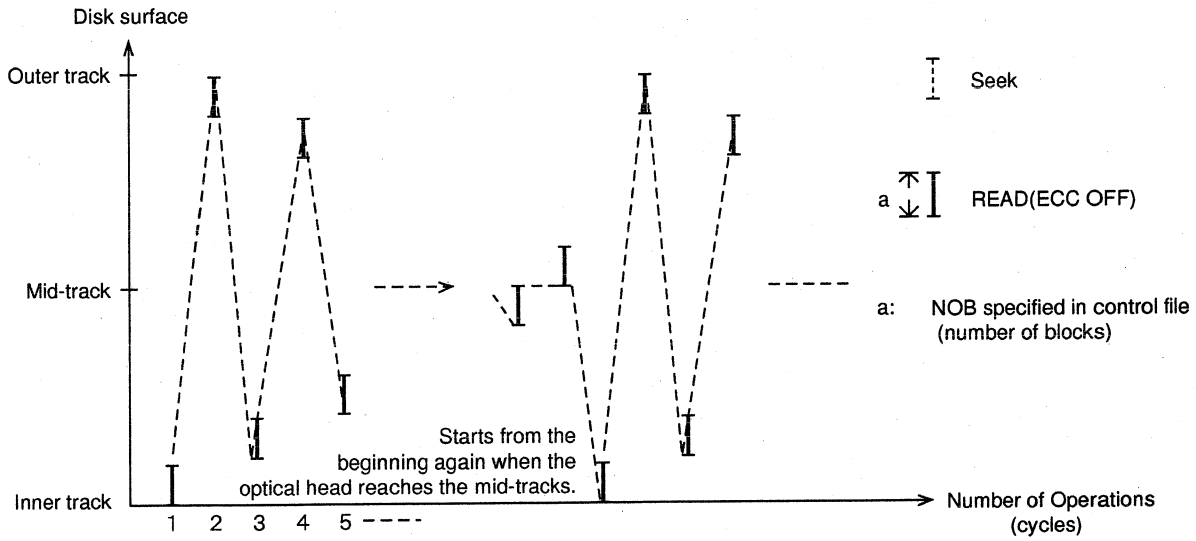


Figure 1

Menu 2: Seek Test [Random]

Reads a random number of blocks beginning from a random logical block address with the READ (Extended, ECC OFF) command (see Figure 2). Data checking and error correction are not performed, only the Seek Test is performed.

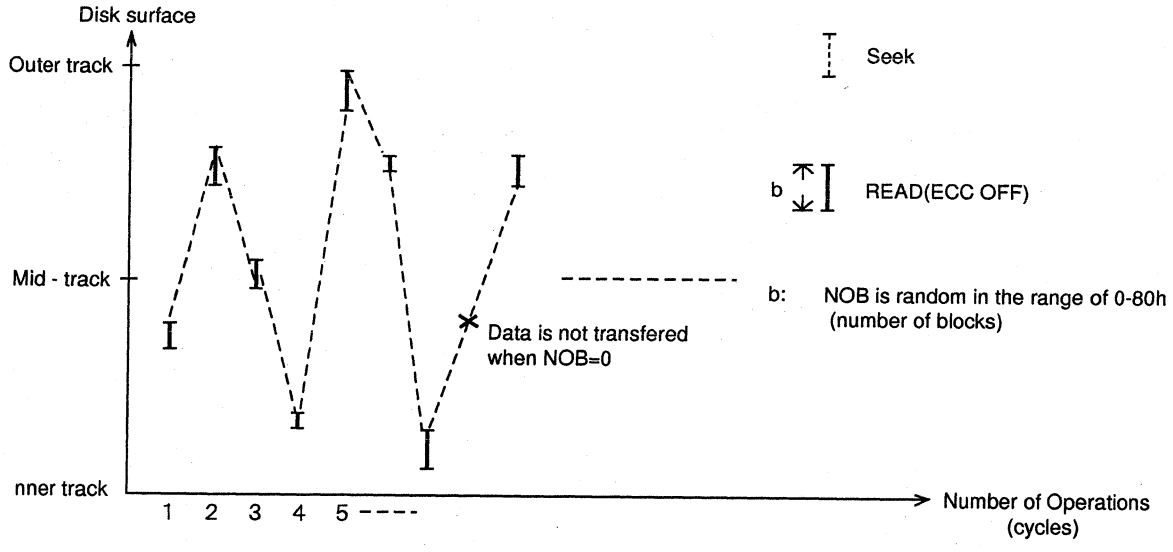


Figure 2

Menu 3: Seek Test [Constant]

Reads the specified number of blocks beginning from the two specified logical block addresses, by alternating between these two specified logical block addresses with the READ (Extended, ECC OFF) command (see Figure 3). Data checking and error correction are not performed, only the Seek Test is performed.

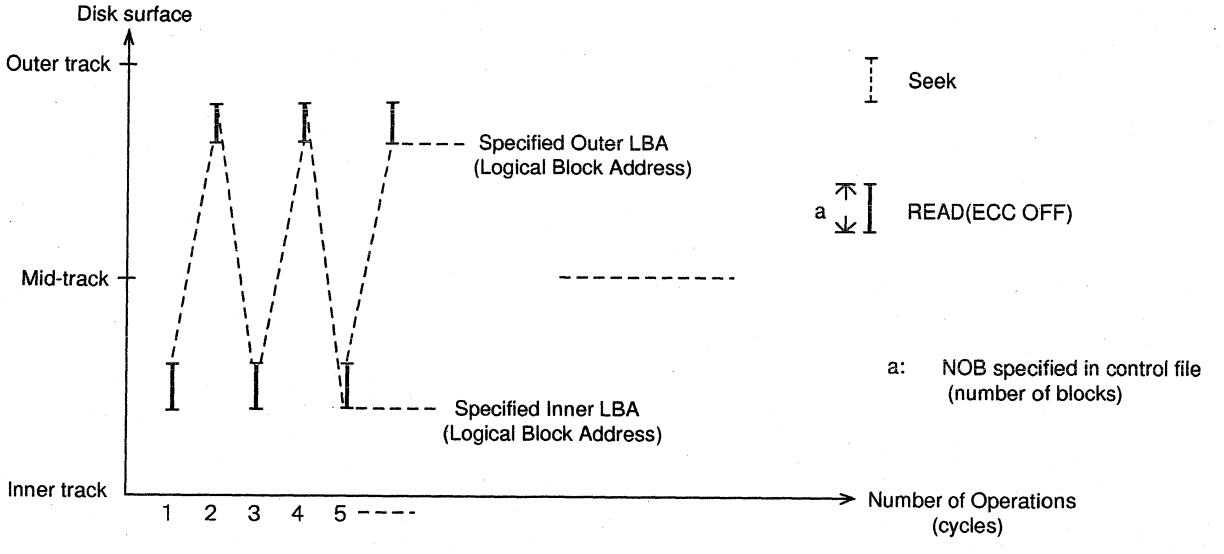


Figure 3

Menu 4: Write and Read Test [Butterfly]

There are two kinds of appropriate operations according to media type, Rewritable and WORM.

(1) Rewritable

Writes the specified number of blocks beginning from the inner tracks and outer tracks and proceeds toward the mid-track, by alternating between the inner tracks and outer tracks with the WRITE (Extended) command. Each time a WRITE command is completed, the area written is read using a READ (Extended, ECC ON) command. The data read is checked by the host computer. If the optical head reaches mid-track, access begins again from the inner tracks and outer tracks (see Figure 4).

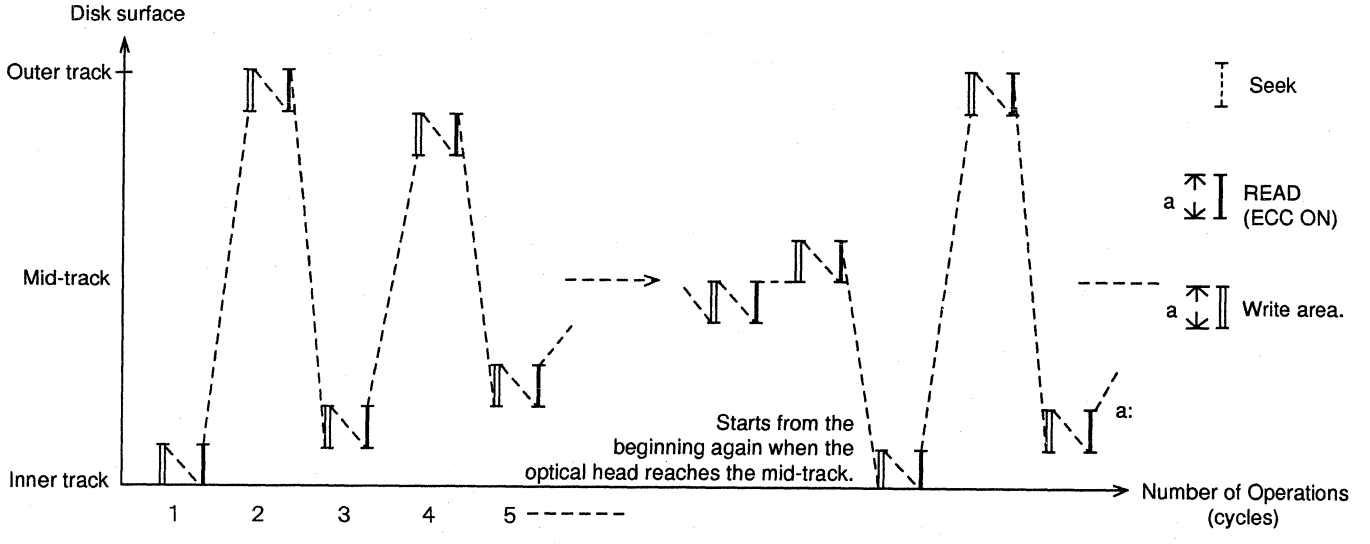


Figure 4

(2) WORM

Writes the specified number of blocks alternating between the inner tracks and outer tracks and proceeds toward the mid-track which are blank, with the WRITE (Extended) command. Each time a WRITE command is completed, the area written is read using a READ (Extended, ECC ON) command. The data read is checked by the host computer. If the blank area is exhausted, the sequence ends (see Figure 5).

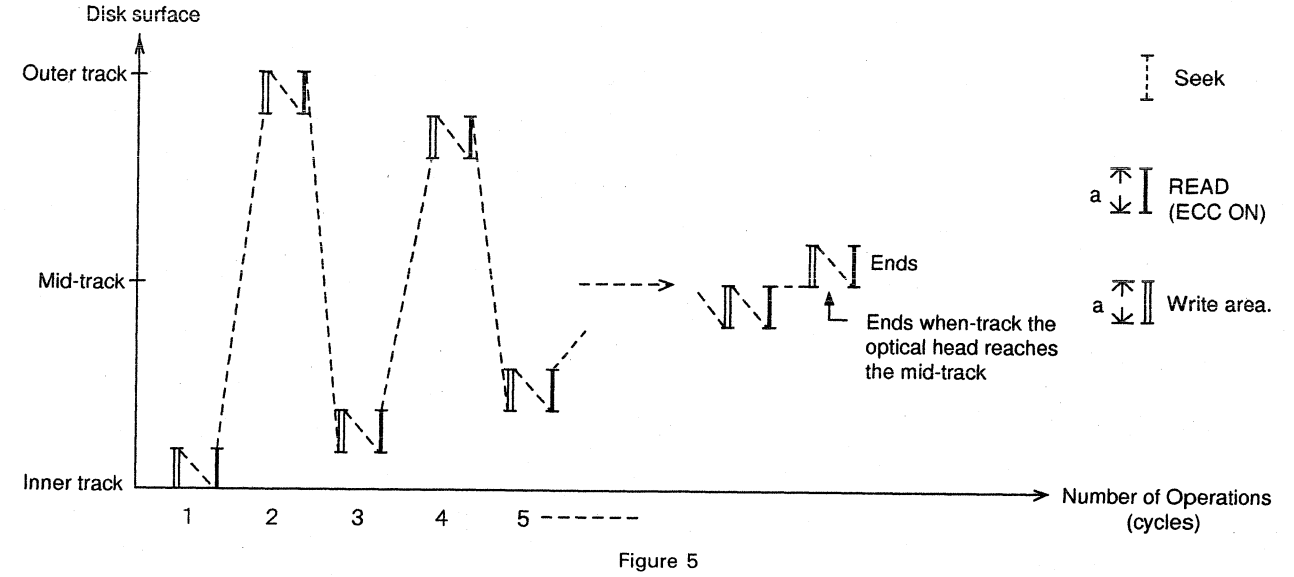


Figure 5

Note: For WORM, writing begins from the inner tracks and outer tracks which are blank.

Menu 5: Write and Read Test [Random]

There are two kinds of appropriate operations according to media type, Rewritable and WORM.

(1) Rewritable

Writes a random number of blocks beginning from a random logical block address with the WRITE (Extended) command. Each time a WRITE command is completed, the area written is read using a READ (Extended, ECC ON) command. The data read is checked by the host computer (see Figure 6).

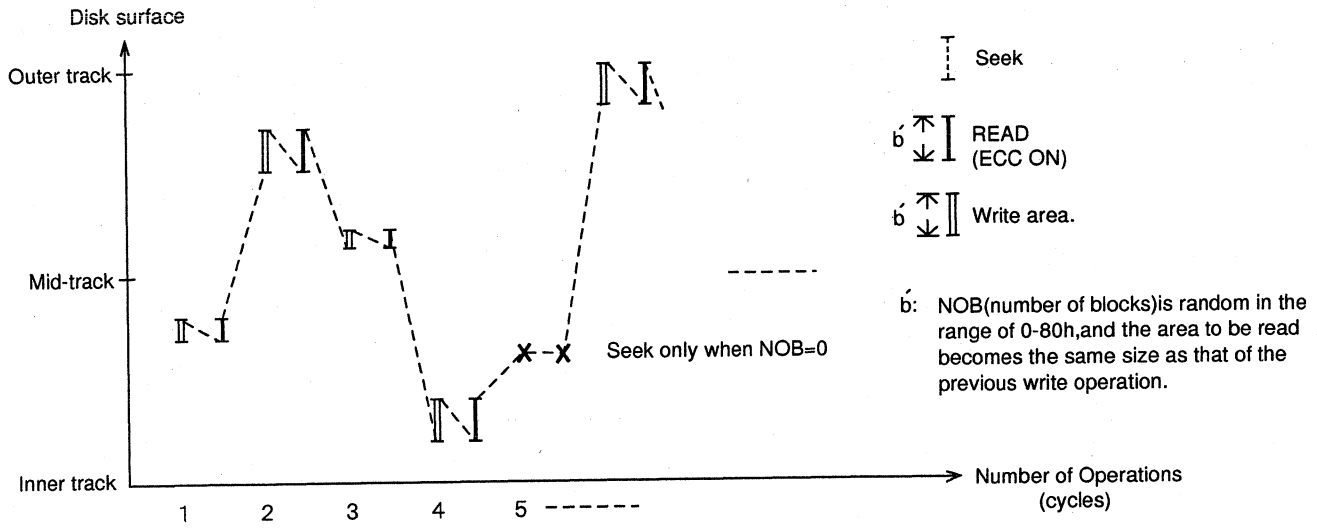


Figure 6

(2) WORM

Seeks to a random logical block address with the SEEK (Extended) command. After that, a random number of blocks are written by alternating from the inner tracks and the outer tracks and proceeding toward the mid-track whick are blank, using a WRITE (Extended) command. The number of blocks for the inner tracks and the corresponding outer tracks are the same. Each time a WRITE command is completed, the area written is read using a READ (Extended, ECC ON) command. The data read is checked by the host computer. If the blank area is exhausted, the sequence ends (see Figure 7).

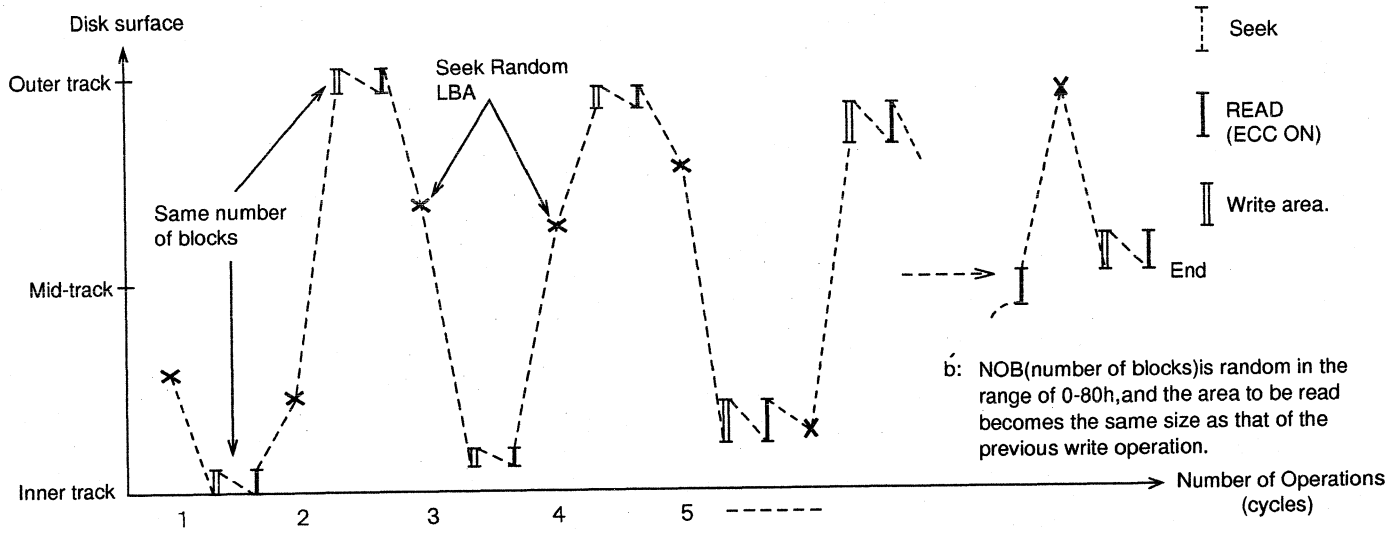


Figure 7

Note: For WORM, writing begins from the inner tracks and outer tracks which are blank.
A pair of inner write operation and outer write operation have the same number of blocks in order to spend the same number of blocks proceeding toward the mid-track.

Menu 6: Write and Read Test [Constant]

The menu is available for only Rewritable.

Writes the specified number of blocks alternating between the two specified logical block addresses with the WRITE (Extended) command. Each time a WRITE command is completed, the area written is read using a READ (Extended, ECC ON) command. The data read is checked by the host computer. (See Figure 8).

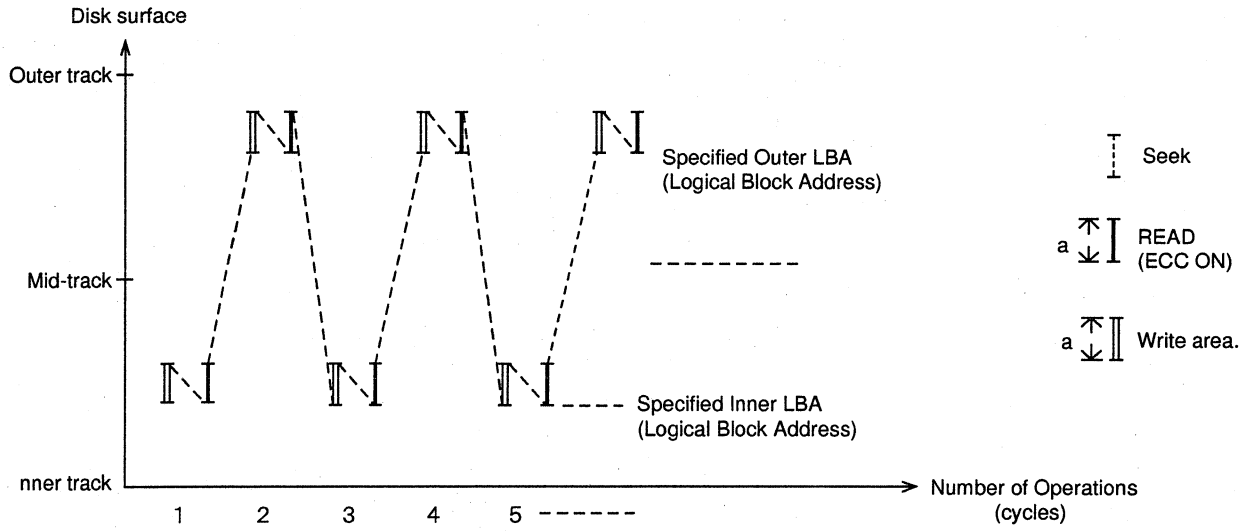


Figure 8

Note: This menu is available only in the Rewritable Mode.

6.4 TESTING FLOW

The test is performed in accordance with the following flowchart.

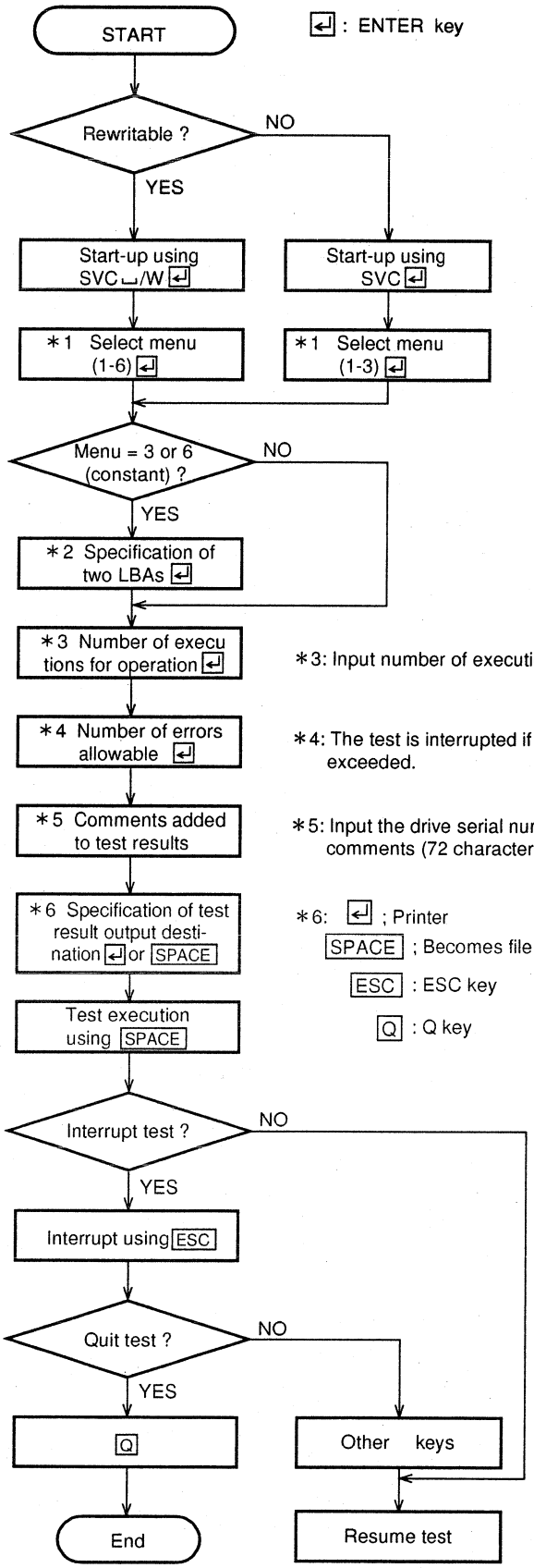
1) Flowchart

1.Test Execution

*1
Menu 1: Seek Test (Read without ECC) [Butterfly]
Menu 2: Seek Test (Read without ECC) [Random]
Menu 3: Seek Test (Read without ECC) [Constant]

Menu 4: Write and Read Test [Butterfly]
Menu 5: Write and Read Test [Random]
Menu 6: Write and Read Test [Constant]

*2: Input LBA (logical block address) in hexadecimal and push ENTER key. There are both inner and outer addresses, so their magnitude is not particularly important.



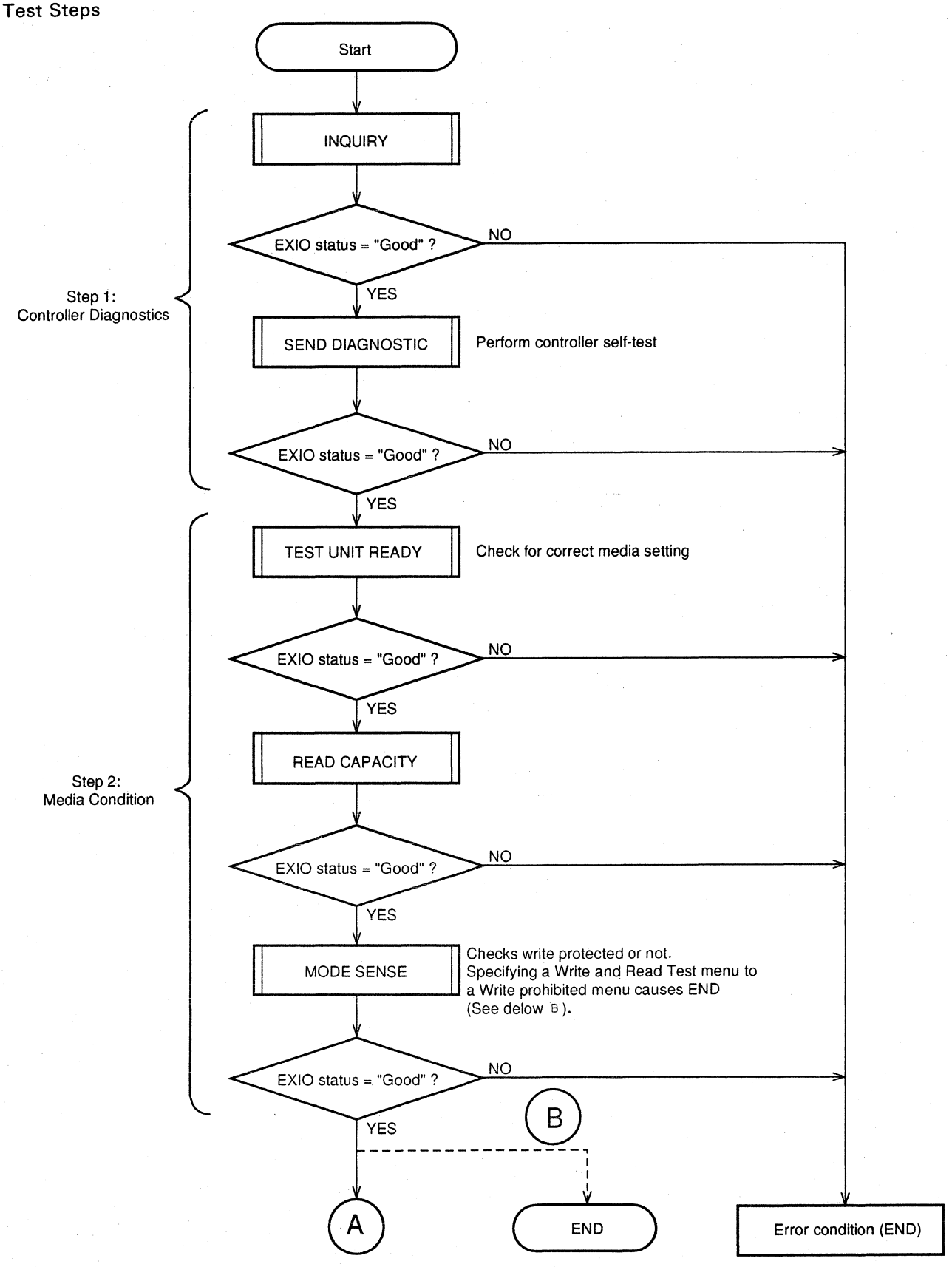
*3: Input number of executions for aging test.

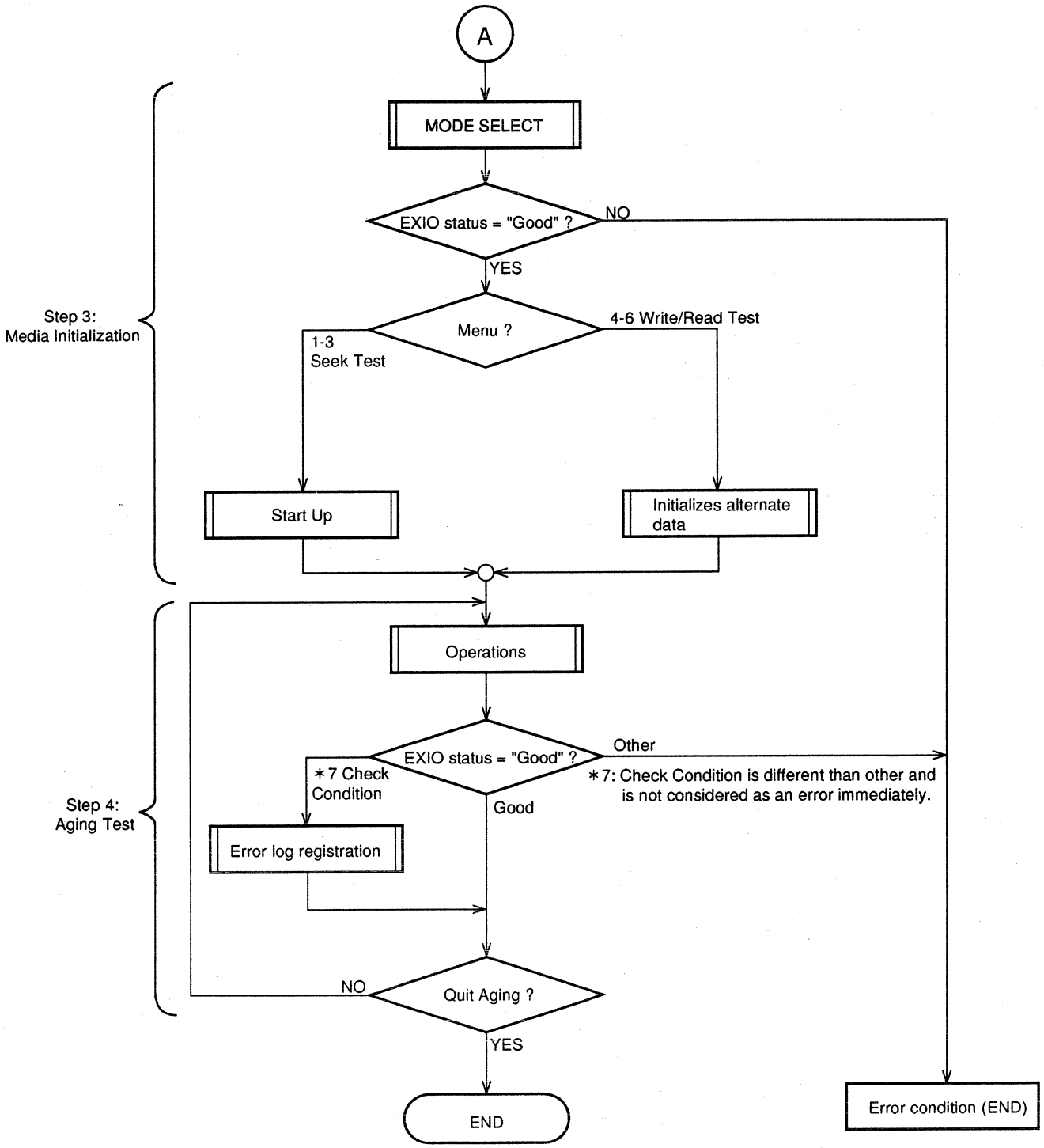
*4: The test is interrupted if the number specified here is exceeded.

*5: Input the drive serial number and optical disk serial number as comments (72 characters or less)

*6: ↵ ; Printer
SPACE ; Becomes file of current drive
ESC : ESC key
Q : Q key

2. Test Steps


Start
INQUIRY
EXIO status = "Good" ?
NO
YES
Step 1:
Controller Diagnostics
SEND DIAGNOSTIC
Perform controller self-test
EXIO status = "Good" ?
NO
YES
TEST UNIT READY
Check for correct media setting
EXIO status = "Good" ?
NO
YES
READ CAPACITY
Step 2:
Media Condition
EXIO status = "Good" ?
NO
YES
MODE SENSE
Checks write protected or not.
Specifying a Write and Read Test menu to
a Write prohibited menu causes END
(See below 'B').
EXIO status = "Good" ?
NO
YES
B
A
END
Error condition (END)


A
MODE SELECT
EXIO status = "Good" ?
NO
YES
Step 3:
Media Initialization
Menu ?
4-6 Write/Read Test
1-3
Seek Test
Start Up
Initializes alternate data
Operations
Step 4:
Aging Test
EXIO status = "Good" ?
Other
∗7 Check Condition
∗7: Check Condition is different than other and is not considered as an error immediately.
Good
Error log registration
NO
Quit Aging ?
YES
END
Error condition (END)

2) Display Messages

6th line of displayed message

"Press [Q] to quit, press other key to continue."
Press [ESC] key during execution to display the above message.
Press [Q] to quit the test. Press any other key to continue.

Pressing [Q] causes "Interrupted by user" to appear momentarily.

"Write operation cannot execute, because write protect tab is set."
The Write and Read Test cannot execute because the write protect tab of the cartridge is set to prohibit write. Press any key to quit the program.

"Complete ····· . Press any key."
Indicates that the specified number of operations have been completed. Press any key to quit the program.

"Fatal Error ····· . Press any key."
If the EXIO status was not "Good" in steps 1-3, or the EXIO status in step 4 was "Good" or these were neither "Check Condition", the test is interrupted and this display appears. Press any key to quit the program.

"Total error count exceeded designated limit. Press any key."
Indicates that the number of allowable errors specified in the Aging Test was exceeded. Press any key to quit the program.

"This WORM disk has no space for write test. Press any key."
This display appears if a Write and Read test was performed using a WORM disk and the blank area was exhausted during the write test. Change to a new disk if this occurs. Press any key to quit the program.

"Cannot write [Const], because this medium is WORM. Press any key."
Displayed if a Write and Read test [Constant] operation is specified for a WORM disk. Press any key to quit the program.

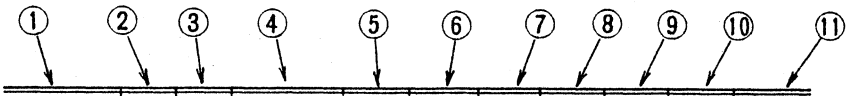
3) Reading the Test Screen

Test results are displayed at each step of the test.

Command Descriptions

①. Command : Displays SCSI command to be executed (blue during execution)
②. LBA : Logical block address for READ, WRITE, or SEEK command
③. NOB : Number of blocks for READ or WRITE, or VERIFY command
④. Distance : Standard movement distance of track when a seek operation included in a READ, WRITE, or SEEK command is executed
⑤. Time : Command execution time, a Warning occurs for a Read or Write of more than 3 seconds
⑥. STS : EXIO status
⑦. SNS : Sense key
⑧. ASC : Additional sense code
⑨. INF : Information Bytes (logical block address where error occurred)
⑩. TFR : Number of bytes actually transferred
⑪. VFY : Data check result (OK/NG)
⑫. Total : Specified number of repeats for aging
⑬. Current : Current number of executions
⑭. Remaining Time: Time remaining until aging complete
⑮. EXIO status display
⑯. Sense key display when error (displayed only when error)
⑰. Additional sense code when error (displayed only when error)

STEP 1: Controller Diagnostics



Command	LBA	NOB	Distance	Time	STS	SNS	ASC	INF	TFR	VFY
INQUIRY	H	H	D	D	0000 H	H	H	H	H	D
S-DIAG	H	H	D	D	H	H	H	H	H	D
	H	H	D	D	H	H	H	H	H	D

⑮ → STS [0000] : Good
⑯ → SNS
⑰ → ASC

STEP 2: Media Condition

Command	LBA	NOB	Distance	Time	STS	SNS	ASC	INF	TFR	VFY
TU READY	H	H	D	D	0000 H	H	H	H	H	D
READ CAP	H	H	D	D	0000 H	H	H	H	H	D
MODE SNS	H	H	D	D	0000 H	H	H	H	H	D

STS [0000] : Good

STEP 3: Media Initialization

Command	LBA	NOB	Distance	Time	STS	SNS	ASC	INF	TFR	VFY
MODE SEL	H	H	D	D	0000 H	H	H	H	H	D
FMT UNIT	H	H	D	D	H	H	H	H	H	D
	H	H	D	D	H	H	H	H	H	D

STS [0000] : Good

STEP 4: Aging Test

⑫ → Total 200 cycle
⑬ → Current 107 cycle
⑭ → Remaining Time 2 min

Command	LBA	NOB	Distance	Time	STS	SNS	ASC	INF	TFR	VFY
WRITE	47604 H	73 H	-7506tr D	0 s D	0000 H	H	H	H	E600 H	D
READ	47604 H	73 H	-3tr D	1 s D	0000 H	H	H	H	E600 H	OK D
	H	H	D	D	H	H	H	H	H	D

STS [0000] : Good

4) EXIO Status and Sense Data

1. EXIO status

Number enclosed in parentheses indicates error code.

- GOOD (0000h)

Indicates that command ended normally.

- CHECK CONDITION (0002h)

Indicates that items that should be reported to the initiator occurred at the time of command execution. The detail references the sense key and additional sense code because this test software automatically issues a REQUEST SENSE command. (However, the sense key is not displayed because there is no error if a sense key BLANK CHECK is caused by the Check Condition during search for an blank area of WORM.)

- BUSY (0008h)

Indicates that specified target is in a Busy condition. If a Busy is returned by the test software, the command is automatically reissued. This display is shown if the Busy condition still exists after 7,000 retries.

- RESERVATION CONFLIST (0018h)

Indicates that the specified target is reserved by another initiator. This does not normally occur with this software.

- CANNOT GET SCSI BUS (0100h)

Indicates that authority to use the SCSI bus could not obtained in the arbitration phase. This does not normally occur with this software.

- NOT BUS FREE (0101h)

Indicates that SCSI bus is in use. If a Not Bus Free is returned by the test software, the command is automatically reissued. This display is shown if the Not Bus Free condition still exists after 7,000 retries.

- SELECTION TIMEOUT (0102h)

Specified target is not connected or no response.

- RESET CONDITION OCCURRED (0103h)

Reset occurred during command execution.

- INVALID COMMAND (1000h)

Command code or parameter specification is incorrect. This does not normally occur with this software.

- SPC DIAGNOSTIC ERROR (8010h)

Error occurred during SPC initialize, or I/O address set value on card and set value during software test disagree.

- SPC PARITY ERROR (5001h)

Parity error occurred during data output to SCSI bus.

- SCSI PARITY ERROR (5003h)

Parity error occurred during data input from SCSI bus.

- SPC ERROR (8000h)

Abnormal SPC internal interrupt occurred.

- INVALID PHASE CHANGE (8100h)

An unexpected phase change occures in the middle of a phase.

- TIMEOUT OR PHASE ERROR (8200h)

Did not proceed to next phase within the required time after completion of a phase, or shifted to an unexpected phase.

- MESSAGE CODE ERROR (8301h)

Undefined message code returned.

- PHASE NOT COMPLETE (8306h)

Does not proceed to Bus Free after command complete.

2. Sense Data in WORM

Number enclosed in parentheses indicates sense key/additional sense code.

- NO SENSE / NO ADDITIONAL SENSE INFORMATION (00h/00h)

Indicates that there is no information to be reported to the initiator. This would be the case for a successful command.

- RECOVERED ERROR / NO ADDITIONAL SENSE INFORMATION (01h/00h)

Indicates that the last READ command completed successfully with retry action by the target. This condition is not considered as an error. The logical block address of the last recovered block is reported in the information bytes of the sense data.

- NOT READY / DRIVE NOT READY (Off Line) (02h/04h)

Indicates that the specified logical unit does not exist.

- NOT READY / MEDIUM NOT PRESENT (02h/80h)

Indicates that no medium has been inserted in the logical unit.

● NOT READY / MODE MISMATCHED (02h /83h)

Indicates that a Rewritable medium is inserted in the logical unit. The initiator may be able to access the medium after issuing the CHANGE MODE command.

● MEDIUM ERROR / WRITE FAULT (03h/03h)

Indicates that a write operation is not completed by the medium defects or by the hardware error of the drive. The logical block address of the first block of which data is not written successfully is reported in the information bytes of the sense data.

● MEDIUM ERROR / DEFECTIVE RECORDED BLOCK OR BLANK BLOCK ENCOUNTERD (03h/11h)

Indicates that the defective recorded block or the blank block was encountered during a read operation. The logical block address of the first block which data is not read successfully is reported in the information bytes of the sense data.

● MEDIUM ERROR / NO DEFECT SPARE LOCATION AVAILABLE (03h/32h)

Indicates that the alternative area for the specified logical blocks on the medium has been exhausted and the write operation was terminated. The logical block address of the first block which data is not written successfully is reported in the information bytes of the sense data.

● HARDWARE ERROR / LOGICAL UNIT COMMUNICATION FAILURE (04h/08h)

Indicates that the last command is terminated by the failure during the communication between the controller and the logical unit.

● HARDWARE ERROR / TRACK FOLLOWING ERROR (04h/09h)

The drive does not correctly trace the track and the command is interrupted.

● HARDWARE ERROR / RAM FAILURE (04h/40h)

Indicates that the RAM diagnostic was failed in the SEND DIAGNOSTIC command or during the controller Power ON self-checking.

● HARDWARE ERROR / DATA PATH DIAGNOSTIC FAILURE (04h/41h)

Indicates that the diagnostics of the error correction and detection circuit were failed in the SEND DIAGNOSTIC command or during the controller Power ON self-checking.

● HARDWARE ERROR / POWER ON DIAGNOSTIC FAILURE (04h/42h)

Indicates that the sum checking of the controller ROM was failed during the controller Power ON self-checking.

● HARDWARE ERROR / MESSAGE REJECT ERROR (04h/43h)

Indicates that the command is terminated by the MESSAGE REJECT message sent from the initiator.

● HARDWARE ERROR / INTERNAL CONTROLLER ERROR (04h/44h)

Indicates that an error is detected during the control of the SCSI interface IC.

● HARDWARE ERROR / INAPPROPRIATE MESSAGE (04h/49h)

Indicates that the command is terminated by the inappropriate message sent from the initiator.

● HARDWARE ERROR / LOADING MECHANISM FAILURE (04h/91h)

Indicates that the medium eject operation was failed by a loading mechanism failure.

● HARDWARE ERROR / DISK MOTOR FAILURE (04h/92h)

Indicates that the rotational speed of the disk motor was not locked.

● HARDWARE ERROR / FOCUSING FAILURE (04h/93h)

Indicates that the focusing servo was not locked during the medium spinning up sequence or focusing servo was failed.

● HARDWARE ERROR / SYNCHRONIZATION ERROR (04h/94h)

Indicates that the synchronization error was detected during the following the tracks.

● HARDWARE ERROR / ID CANNOT BE DETECTED (04h/95)

Indicates that the ID address of the medium could not be detected.

● HARDWARE ERROR / DEFECT MANAGEMENT TRACK NOT EXIST (04h/96h)

Indicates that the Defect Management Track of the WORM medium has not been recorded.

- HARDWARE ERROR / CONTROL TRACK READ FAILURE (04h/97h)

Indicates that the control track has not been read by the target because of any hardware failures of the drive or the invalid medium is inserted logical unit.

- HARDWARE ERROR / INVALID CODE IS RETURNED FROM THE LOGICAL UNIT (04h/98h)

Indicates that the inappropriate status was returned from the logical unit.

- ILLEGAL REQUEST / INVALID OPERATION CODE (05h/20h)

Indicates that the invalid SCSI command which is not implemented or which is in inappropriate use is issued by the initiator.

- ILLEGAL REQUEST / ILLEGAL LOGICAL BLOCK ADDRESS (05h/21h)

Indicates that the logical block address specified in CDB is out of the medium capacity. The informaion bytes of the sense data always indicate the first logical block address which exceeds the user capacity (the last logical block address of the medium plus one).

- ILLEGAL REQUEST / ILLEGAL FIELD IN CDB (05h/24h)

Indicates that the invalid codes or bits are set in CDB.

- ILLEGAL REQUEST / INVALID LUN (05h/25h)

Indicates that the logical unit number set in CDB is invalid.

- ILLEGAL REQUEST / INVALID FIELD IN PARAMETER LIST (05h/26h)

Indicates that the invalid codes or bits are set in the parameter list sent by the initiator during the DATA OUT phase.

- ILLEGAL REQUEST / COPY CANNOT EXECUTE SINCE HOST CANNOT DISCONNECT (05h/2Bh)

Indicates that the copy operation cannot be performed because the initiator does not have the disconnect capability.

- UNIT ATTENTION / MEDIUM CHANGED (06h/28h)

Indicates that the medium in the logical unit has been changed.

- UNIT ATTENTION / POWER ON OR RESET OR BUS DEVICE RESET IS OCCURRED (06h/29h)

Indicates that the power is turned on. It also indicates that the target has been reset by the SCSI bus RST signal is true or by the BUS DEVICE RESET message sent from the initiator.

- UNIT ATTENTION / MODE SELECT PARAMETERS ARE CHANGED (06h/2Ah)

Indicates that the MODE SELECT parameters have been changed by the MODE SELECT command sent from another initiator.

- UNIT ATTENTION / CONTROLLER MODE IS CHANGED (06h/85h)

Indicates that the controller mode has been changed by the CHANGE MODE command sent from another initiator.

- DATA PROTECT / WRITE PROTECTED (07h/27h)

Indicates that the write-protect tab on the cartridge in the logical unit is set to the write-protected.

- DATA PROTECT / COPY CANNOT EXECUTE BECAUSE OF THE RESERVATION (07h/82h)

Indicates that the copy operation is inhibited because all or a part of the logical blocks specified in the COPY command are reserved by another initiator.

- BLANK CHECK / NO ADDITIONAL SENSE INFORMATION (08h/00h)

Indicates that the target encountered a nonblank block while blank checking of a VERIFY command (the BlkVfy bit is set to one),or while blank checking of a write operation (the EBC bit in the MODE SELECT parameter is set to one).
When the RDBC bit in the MODE SELECT parameter is set to one,it also indicates that a blank block was found during a read operation.

- ABORTED COMMAND / SCSI INTERFACE PARITY ERROR (0Bh/47h)

Indicates that the target detects the parity error and aborts the command after a retry attempt.

- ABORTED COMMAND / INITIATOR DETECTED ERROR (0Bh/48h)

Indicates that the target receives the INITIATOR DETECTED ERROR message from the initiator and aborts the command after a retry attempt.

3. Sense Data in Rewritable

Number enclosed in parentheses indicates sense key/additional sense code.

- NO SENSE / NO ADDITIONAL SENSE INFORMATION (00h/00h)

Indicates that there is no information to be reported to the initiator. This would be the case for a successful command.

- RECOVERED ERROR / NO ADDITIONAL SENSE INFORMATION (01h/00h)

Indicates that the last READ command completed successfully with retry action by the target. This condition is not considered as an error. The logical block address of the last recovered block is reported in the information bytes of the sense data.

- NOT READY / DRIVE NOT READY (Off Line) (02h/04h)

Indicates that the specified logical unit dose not exist.

- NOT READY / MEDIUM NOT PRESENT (02h/80h)

Indicates that no medium has been inserted in the logical unit.

- NOT READY / MODE MISMATCHED (02h/83h)

Indicates that a WORM medium is inserted in the logical unit. The initiator may be able to access the medium after issuig the CHANGE MODE command.

- MEDIUM ERROR / WRITE FAULT (03h/03h)

Indicates that a write operation is not completed by the medium defects or by the hardware error of the drive. The logical block address of the first block which data is not written successfully is reported in the information bytes of the sense data.

- MEDIUM ERROR / DEFECTIVE RECORDED BLOCK OR ERASED BLOCK ENCOUNTERED (03h/11h)

Indicates that the defective recorded block or the erased block was encountered during a read operation. The logical block address of the first block which data is not read successfully is reported in the information bytes of the sense data.

- MEDIUM ERROR / MEDIUM FORMAT CORRUPTED (03h/31h)

Indicates that the invalid medium is inserted in the logical unit.

- MEDIUM ERROR / NO DEFECT SPARE LOCATION AVAILABLE (03h/32h)

Indicates that the alternative area for the specified logical blocks on the medium has been exhausted and the write operation was terminated. The logical block address of the first block which data is not written successfully is reported in the information bytes of the sense data.

- MEDIUM ERROR / UNFORMATTED MEDIUM (03h/84h)

Indicates that the Defect Management Track of the rewritable medium in the logical unit has not been recorded and a medium access operations are dis-abled. The initiator may be able to request the target to record the defect management information to the Defect Management Track by issuing the FORMAT UNIT command.

- HARDWARE ERROR / LOGICAL UNIT COMMUNICATION FAILURE (04h/08h)

Indicates that the last command is terminated by the failure during the communication between the controller and the logical unit.

- HARDWARE ERROR / TRACK FOLLOWING ERROR (04h/09h)

The drive does not correctly trace the track and the command is interrupted.

- HARDWARE ERROR / RAM FAILURE (04h/40h)

Indicates that the RAM diagnostic was failed in the SEND DIAGNOSTIC command or during the controller Power ON self-checking.

- HARDWARE ERROR / DATA PATH DIAGNOSTIC FAILURE (04h/41h)

Indicates that the diagnostics of the error correction and detection circuit were failed in the SEND DIAGNOSTIC command or during the controller Power ON self-checking.

- HARDWARE ERROR / POWER ON DIAGNOSTIC FAILURE (04h/42h)

Indicates that the sum checking of the controller ROM was failed during the controller Power ON self-checking.

- HARDWARE ERROR / MESSAGE REJECT ERROR (04h/43h)

Indicates that the command is terminated by the MESSAGE REJECT message sent from the initiator.

- HARDWARE ERROR / INTERNAL CONTROLLER ERROR (04h/44h)

Indicates that an error is detected during the control of the SCSI interface IC.

- HARDWARE ERROR / INAPPROPRIATE MESSAGE (04h/49h)

Indicates that the command is terminated by the inappropriate message sent from the initiator.

- HARDWARE ERROR /LOADING MECHANISM FAILURE (04h/91h)

Indicates that the medium eject operation was failed by a loading mechanism failure.

- HARDWARE ERROR / DISK MOTOR FAILURE (04h/92h)

Indicates that the rotational speed of the disk motor was not locked.

- HARDWARE ERROR / FOCUSING FAILURE (04h/93h)

Indicates that the focusing servo was not locked during the medium spinning up sequence or focusing servo was failed.

- HARDWARE ERROR / SYNCHRONIZATION ERROR (04h/94h)

Indicates that the synchronization error was detected during the following the tracks.

- HARDWARE ERROR / ID CANNOT BE DETECTED (04h/95h)

Indicates that the ID address of the medium could not be detected.

- HARDWARE ERROR / CONTROL TRACK READ FAILURE (04h/97h)

Indicates that the control track has not been read by the target because of any hardware failures of the drive.

- HARDWARE ERROR / INVALID CODE IS RETURNED FROM THE LOGICAL UNIT (04h/98h)

Indicates that the inappropriate status was returned from the logical unit.

- ILLEGAL REQUEST / INVALID OPERATION CODE (05h/20h)

Indicates that the invalid SCSI command which is not implemented or which is in inappropriate use is issued by the initiator.

- ILLEGAL REQUEST / ILLEGAL LOGICAL BLOCK ADDRESS (05h/21h)

Indicates that the logical block address specified in CDB is out of the medium capacity. The information bytes of the sense data always indicate the first logical block address which exceeds the user capacity (the last logical block address of the medium plus one).

- ILLEGAL REQUEST / ILLEGAL FIELD IN CDB (05h/24h)

Indicates that the invalid codes or bits are set in CDB.

- ILLEGAL REQUEST / INVALID LUN (05h/25h)

Indicates that the logical unit number set in CDB is invalid.

- ILLEGAL REQUEST / INVALID FLELD IN PARAMETER LIST (05h/26h)

Indicates that the invalid codes or bits are set in the parameter list sent by the initiator during the DATA OUT phase.

- ILLEGAL REQUEST / COPY CANNOT EXECUTE SINCE HOST CANNOT DISCONNECT (05h/2Bh)

Indicates that the copy operation cannot be performed because the initiator does not have the disconnect capability.

- UNIT ATTENTION / MEDIUM CHANGED (06h/28h)

Indicates that the medium in the logical unit has been changed.

- UNIT ATTENTION / POWER ON OR RESET OR BUS DEVICE RESET IS OCCURRED (06h/29h)

Indicates that the power is turned on. It also indicates that the target has been reset by the SCSI bus RST signal is true or by the BUS DEVICE RESET message sent from the initiator.

- UNIT ATTENTION / MODE SELECT PARAMETERS ARE CHANGED (06h/2Ah)

Indicates that the MODE SELECT parameters have been changed by the MODE SELECT command sent from another initiator.

- UNIT ATTENTION / CONTROLLER MODE IS CHANGED (06h/85h)

Indicates that the controller mode has been changed by the CHANGE MODE command sent from another initiator.

- DATA PROTECT / WRITE PROTECTED (07h/27h)

Indicates that the write-protect tab on the cartridge in the logical unit is set to the write-protected.

- DATA PROTECT / COPY CANNOT EXECUTE BECAUSE OF THE RESERVATION (07h/82h)

Indicates that the copy operation is inhibited because all or a part of the logical blocks specified in the COPY command are reserved by another initiator.

- ABORTED COMMAND / SCSI INTERFACE PARITY ERROR (0Bh/47h)

Indicates that the target detects the parity error and aborts the command after a retry attempt.

- ABORTED COMMAND / INITIATOR DETECTED ERROR (0Bh/48h)

Indicates that the target receives the INITATOR DETECTED ERROR message from the initiator and aborts the command after a retry attempt.

6.5 READING TEST RESULTS

Test results are displayed as shown below.

********** Aging Report **********

Total 117 cycle 3 min ..... Actual number of cycles executed and total execution time

Total Error Count=1 ..... Total number of errors

Total Warning Count=2 ..... Total number of warnings

****

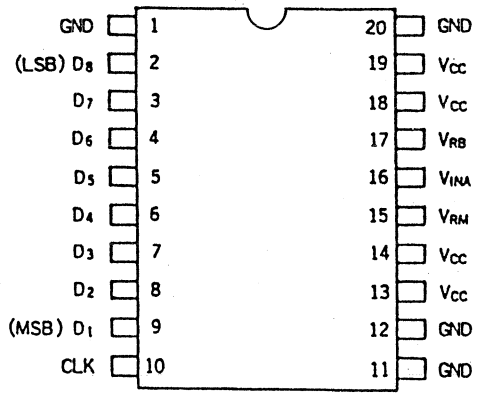
7. IC INFORMATION

- *The information shown in the list is basic information and may not correspond exactly to that shown in the schematic diagrams.*

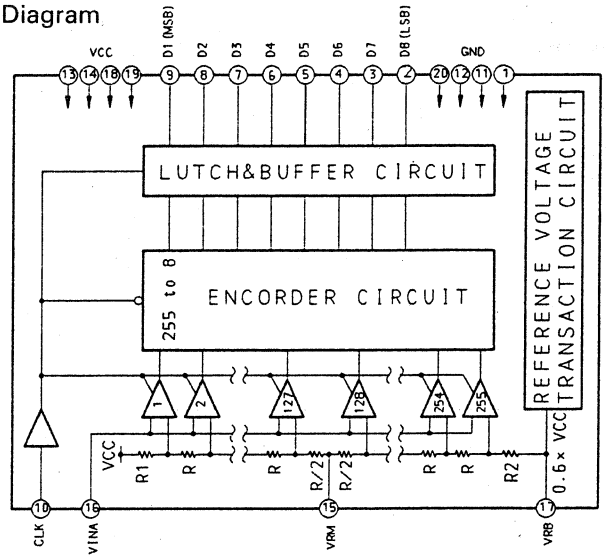
■ MB40558PF (IC105 : MAIN BOARD ASSY B)

● A/D Converter

- Pin Assignment (Top View)



- Block Diagram



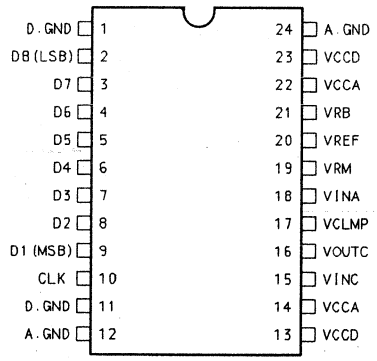
- Pin Function

No.	Function	I/O	Name	Description
1	GND	–	GND	Ground terminal
2 | 9	D8 | D1	O	Digital Signal Output	The output voltage is TTL level. (D1: MSB, D8: LSB)
10	CLK	I	Clock Input	The input voltage is TTL level.
11 12	GND	–	GND	Ground terminal
13 14	Vcc	–	Power Supply	+5 V Power supply
15	VRM	O	Intermediate voltage output	The intermediate potential of Vcc and VRB is put out (4 V).
16	VINA	I	Analog Signal Input	The input range is from VRB to Vcc (3 V to 5 V).
17	VRB	O	Reference Voltage Output	0.6 × Vcc (V) is put out (3 V).
18 19	Vcc	–	Power Supply	Connected to power supply.
20	GND	–	GND	Ground terminal

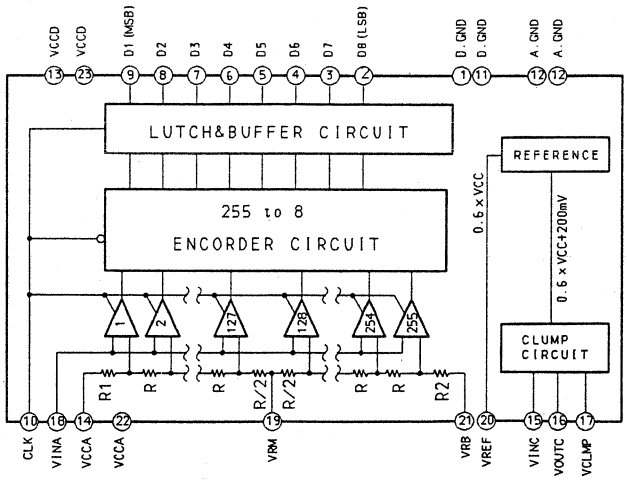
■ MB40568PF−25 (IC151 : MAIN BOARD ASSY B)

● A/D Convereter

● Pin Assignment (Top View)



● Block Diagram



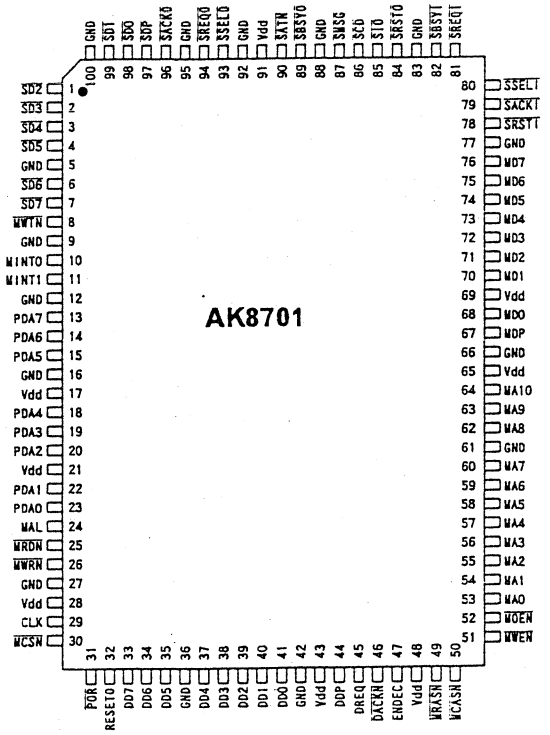
● Pin Function

No.	Pin Name	Description
1	D. GND	Digital ground terminal.
2 | 9	D8 | D1	Digital signal output terminal
10	CLK	Clock input terminal
11	D. GND	Digital ground terminal.
12	A. GND	Analog ground terminal.
13	VCCD	Power supply voltage impression terminal.
14	VCCA	Power supply voltage impression terminal.
15	VINC	Clamp circuit input terminal.
16	VOUTC	Clamp circuit output terminal.
17	VCLMP	Clamp circuit output terminal.
18	VINA	Analog input terminal
19	VRM	Reference voltage monitor terminal.
20	VREF	Reference voltage output terminal.
21	VRB	Power supply analog voltage impression terminal.
22	VCCA	Power supply voltage impression terminal.
23	VCCD	Power supply voltage impression terminal.
24	A. GND	Analog ground terminal.

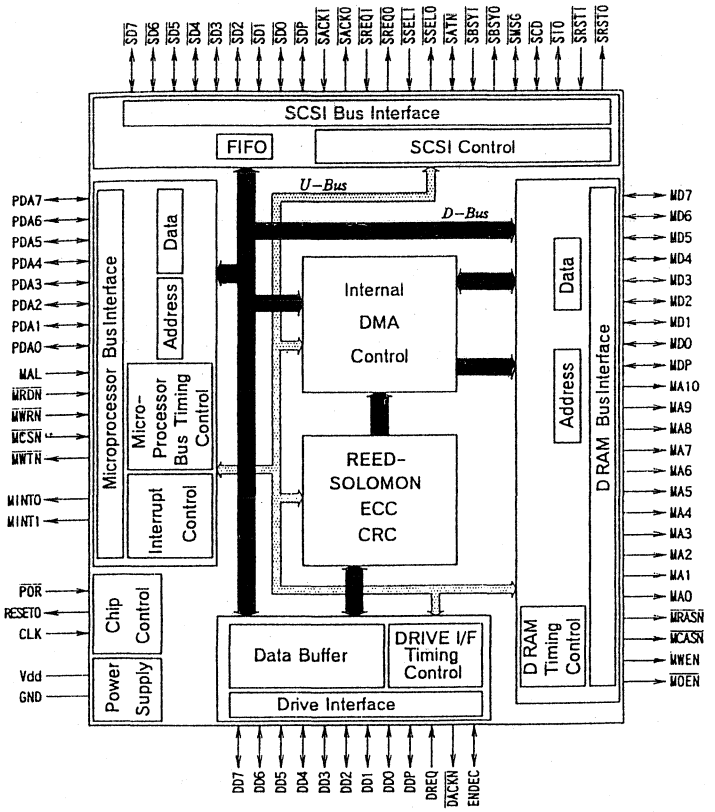
■ AK8701 (IC337 : MAIN BOARD ASSY B)

● SCSI Controller

● Pin Assignment (Top View)



● Block Diagram



● Pin Function

No.	Pin Name	I/O	Description
1 | 4	$\overline{SD2}$ | $\overline{SD5}$	I/O	SCSI data bit2 | SCSI data bit5
5	GND	–	
6	$\overline{SD6}$	I/O	SCSI data bit6
7	$\overline{SD7}$	I/O	SCSI data bit7 (MSB)
8	$\overline{MWTN}$	O	Wait output in regard to the microcomputer
9	GND	–	
10	MINT0	O	Interrupt signal output in regard to the SCSI
11	MINT1	O	Interrupt signal output by a cause other than SCSI
12	GND	–	
13 | 15	PAD7 | PAD5	I/O	μ-com • address/data • bit7 | μ-com • address/data • bit5

No.	Pin Name	I/O	Description
16	GND	–	
17	Vdd	–	
18 | 20	PAD4 | PAD2	I/O	μ-com • address/data • bit4 | μ-com • address/data • bit2
21	Vdd	–	
22	PAD1	I/O	μ-com • address/data • bit1
23	PAD0	I/O	μ-com • address/data • bit0
24	MAL	I	Input of the microcomputer • address latch enable signal
25	$\overline{MRDN}$	I	Input of the microcomputer • read • strobe signal
26	$\overline{MWRN}$	I	Input of the microcomputer • write • strobe signal
27	GND	–	

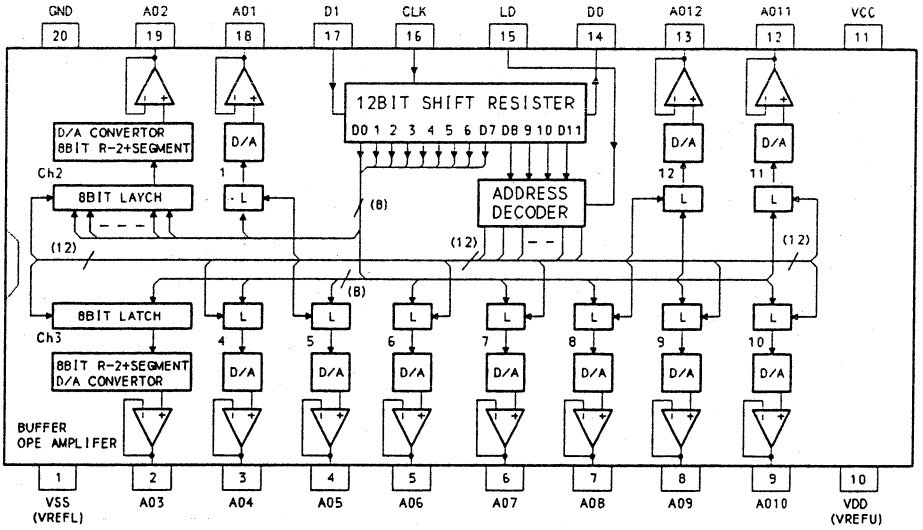
No.	Pin Name	I/O	Description
28	Vdd	–	
29	CLK	I	Input of the basic clock of the chip
30	$\overline{\text{MCSN}}$	I	Chip select signal. This becomes "Low" with register access from the microcomputer.
31	$\overline{\text{POR}}$	I	Reset signal input for initialization of this entire chip.
32	RESETO	O	Becomes active under one of the following conditions. When the POR signal is active or when the SCSI reset signal is active and reset has not been serviced.
33 | 35	DD7 | DD5	I/O	ENDEC interface data bit7 (MSB) | ENDEC interface data bit5
36	GND	–	
37 | 41	DD4 | DD0	I/O	ENDEC interface data bit4 | ENDEC interface data bit0
42	GND	–	
43	Vdd	–	
44	DDP	I/O	ENDEC interface parity bit (option)
45	DREQ	I	Data request signal from ENDEC
46	$\overline{\text{DACKN}}$	O	Data strobe signal answering DREQ
47	ENDEC	I/O	When set to output mode, output is made at the time of completion of transmission of the data of one sector (600 byte). When set to input mode, enter an active signal at the time of completion of transmission of the data of one sector.
48	Vdd	–	
49	$\overline{\text{MRASN}}$	O	DRAM row address strobe
50	$\overline{\text{MCASN}}$	O	DRAM column address strobe
51	$\overline{\text{MWEN}}$	O	DRAM write enable
52	$\overline{\text{MOEN}}$	O	DRAM output enable
53 | 60	MA0 | MA7	O	DRAM address bit0 | DRAM address bit7
61	GND	–	
62 | 64	MA8 | MA10	O	DRAM address bit8 | DRAM address bit10 (MSB)

No.	Pin Name	I/O	Description
65	Vdd	–	
66	GND	–	
67	MDP	I/O	DRAM data parity bit (option)
68	MD0	I/O	DRAM data bit0
69	Vdd	–	
70 | 76	MD1 | MD7	I/O	DRAM data bit1 | DRAM data bit7
77	GND	–	
78	$\overline{\text{SRSTI}}$	I	SCSI RST (Reset) signal
79	$\overline{\text{SACKI}}$	I	SCSI ACK (Acknowledge) signal
80	$\overline{\text{SSELI}}$	I	SCSI SEL (Select) signal
81	$\overline{\text{SREQI}}$	I	SCSI REQ (Request) signal
82	$\overline{\text{SBSYI}}$	I	SCSI BSY (Busy) signal
83	GND	–	
84	$\overline{\text{SRSTO}}$	O	SCSI RST (Reset) signal
85	$\overline{\text{SIO}}$	I/O	SCSI I/O (Input/Output) signal
86	$\overline{\text{SCD}}$	I/O	SCSI C/D (Command/Data) signal
87	$\overline{\text{SMSG}}$	I/O	SCSI MSG (Message) signal
88	GND	–	
89	$\overline{\text{SBSYO}}$	O	SCSI BSY (Busy) signal
90	$\overline{\text{SATN}}$	I/O	SCSI ATN (Attention) signal
91	Vdd	–	
92	GND	–	
93	$\overline{\text{SSELO}}$	O	SCSI SEL (Select) signal
94	$\overline{\text{SREQO}}$	O	SCSI REQ (Request) signal
95	GND	–	
96	$\overline{\text{SACKO}}$	O	SCSI ACK (Acknowledge) signal
97	$\overline{\text{SDP}}$	I/O	SCSI data • parity bit (option)
98	$\overline{\text{SD0}}$	I/O	SCSI data bit0 (LSB)
99	$\overline{\text{SD1}}$	I/O	SCSI data bit1
100	GND	–	

■ M62352GP (IC129 : MAIN BOARD ASSY B)

● D/A Converter

● Block Diagram



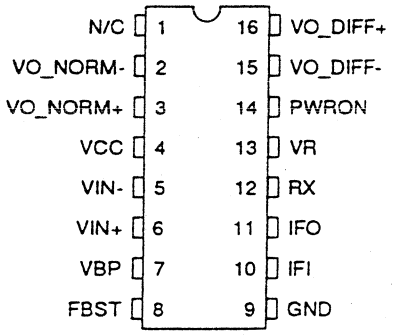
● Pin Function

No.	Symbol	Description
1	Vss	DA converter lower side reference voltage (VrefL) input terminal
2 | 9	AO3 | AO10	8 bit DA output
10	VDD	DA converter upper side reference voltage (VrefU) input terminal
11	Vcc	Power supply terminal
12	AO11	8 bit DA output
13	AO12	
14	D0	12 bit shift register MSB bit data output
15	LD	With input of High level to the LD terminal, the value of the 12 bit shift register is decoded and loaded into the D/A output register.
16	CLK	Shift clock input terminal. With rise of the shift clock, the input signal from the DI terminal is given as input to the 12 bit shift register.
17	DI	Serial data input terminal. Input of serial data with a data length of 12 bits.
18	AO1	8 bit DA output
19	AO2	
20	GND	GND terminal

■ GGC1087 (IC160 : MAIN BOARD ASSY B) (SSI32F8020A−CN)

● Programmable Filter IC

● Pin Assignment (Top View)



● Pin Function

No.	Name	Description
1	N/C	NOT CONNECT
2	VO NORM−	DIFFERENTIAL NORMAL OUTPUTS.
3	VO NORM+	
4	VCC	+5V SUPPLY
5	VIN−	DIFFERENTIAL NORMAL OUTPUTS.
6	VIN+	
7	VBP	FREQUENCY BOOST PROGRAM INPUT. The slimmer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VR. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VR and GND. No boost is applied if the FBST pin is grounded, or at logic low.
8	FBST	FREQUENCY BOOST. A high logic level or open input enables the frequency boost circuitry. No boost is applied if the FBST pin is grounded, or at logic low.
9	GND	GROUND
10	IFI	FREQUENCY PROGRAM INPUT. The filter cutoff frequency fc, is set by an external current IFI, injected into this pin. IFI must be proportional to current IFO. This current can be set with an external current generator such as a DAC, referenced to IFO.

No.	Name	Description
11	IFO	PTAT CURRENT REFERENCE OUTPUT. This pin outputs a PTAT reference current which is externally scaled for control input into IFI.
12	RX	PTAT REFERENCE CURRENT SET. PTAT (proportional to absolute temperature) reference current IFO is equivalent to the current set on this pin.
13	VR	REFERENCE VOLTAGE. Internally generated reference voltage.
14	PWRON	POWER ON. A high logic level circuit enebles the chip. A low level puts the chip in a low power state. A low or open circuit disables the chip.
15	VO DIFF−	DIFFERENTIAL OUTPUTS.
16	VO DIFF+	

■ PD6132A (IC147 : MAIN BOARD ASSY B)

● Digital Servo IC

● Pin Function

No.	Pin Name	I/O	Buffer Name
1	VDD	–	
2 | 8	PAD0 | PAD6	I	I2B
9	VSS	–	
10	PAD7	I	I2B
11	EGEI	I	I2B
12	SSMR	O	O2P
13	PBCLP	O	O2P
14	MCLP1	O	O2P
15	MCLP2	O	O2P
16	PPMO1	O	O2P
17	SBGATE	O	O2P
18	VDD	–	
19	VSS	–	
20	XTS0	I	I2BU
21	XTS1	I	I2BU
22 | 29	TD0 | TD7	O	O2P
30	VSS	–	
31	XTS2	I	I2BU
32	SRDATA	O	O2P
32	SRDATA	O	O2P
33	SCK	O	O2P
34	SCSSLT	O	O2P
35	XREFEDGE	O	O2P
36	XACTEDGE	O	O2P
37 | 44	FD0 | FD7	O	O2P
45	VSS	–	
46	PCK	I	ILB
48 | 53	A0 | A6	I	I2B
54	VDD	–	
55	VSS	–	
56	A7	I	I2B
57 | 64	D0 | D7	I/O	H8TF

No.	Pin Name	I/O	Buffer Name
65	CPUCK	I	I2B
66	VSS	–	
67	EXSYNC	I	ILB
68	XEXTTRK	I	I2B
69	PHLATE	O	O2P
70	PHEARLY	O	O2P
71	FDWREQ	O	O2P
72	FUPREQ	O	O2P
73	VDD	–	
74	SPFG	I	I2B
75	TSO0	O	O2P
76	XIDINT	O	O2P
77	XWR	I	I2B
78	XRD	I	I2B
79	FETCS0	O	O2P
80	FETCS1	O	O2P
81	VSS	–	
82 | 87	FETCS2 | FETCS7	O	O2P
88	LCATED1	O	O2P
89	LCATED2	O	
90	VDD	–	
91	VSS	–	
92 | 97	LCATED3 | LCATED8	O	O2P
98	WGT2	I	I2B
99	TSMR	I	I2B
100	SYDX	O	O2P
101	XINT1	O	O2P
102	VSS	–	
103	HEAD415	O	O2P
104	M1FOK	O	O2P
105	SYOK	O	O2P
106	FSOK	O	O2P
107	EGT	O	O2P
108	LGT	O	O2P

No.	Pin Name	I/O	Buffer Name
109 | 116	AD0 | AD7	I	I2B
117	VSS	–	
118	BUCK	O	O2P
119	XWRCLK	O	O2P
120	FESEL	O	O2P
121	FSFG	O	O2P
122	XSEGMT0	O	O2P
123	TSCKEN	I	IKBU
124	XCKMASS	I	ILB
125	XCK415	I	ILB
126	VDD	–	
127	VSS	–	
128	MASS	O	O2P
129	XMASS	O	O2P
130	XRST	I	ILB
131	XBMALM	I	I2B
132	XLMALM	I	I2B
133	REFCH	O	O2P
134	DIFR	O	O2P
135	TE1EDGE	O	O2P
136	T4EDGE	O	O2P
137	T16EDGE	O	O2P
138	VSS	–	
139	T64EDGE	O	O2P
140	XJKB	O	O2P
141	XEN	O	O2P
142	XTLOK	O	O2P
143	XFLSW	O	O2P
144	TAS	O	O2P

■ PD6133A (IC328 : MAIN BOARD ASSY B)

● Read/Write IC

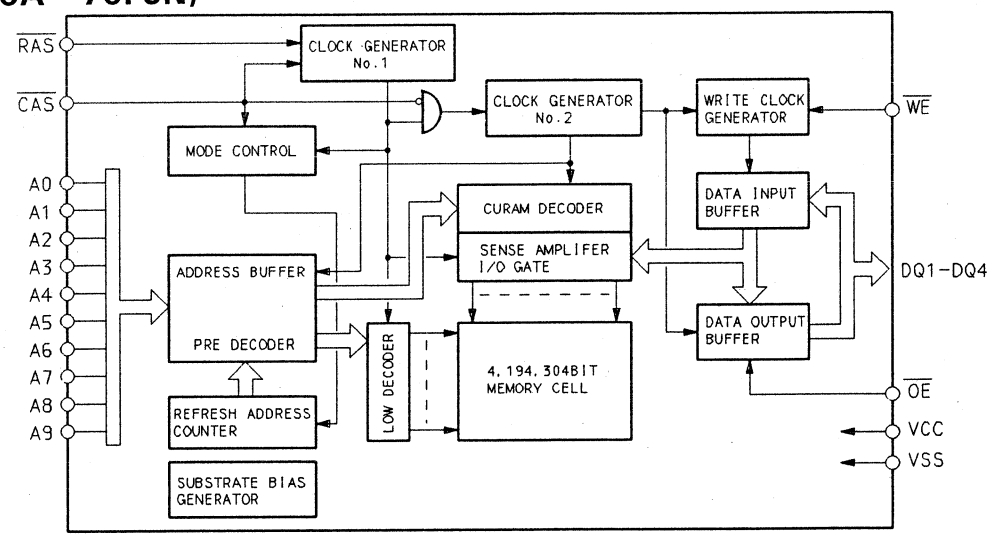
● Pin Function

No.	Pin Name	I/O	Buffer Name
1	A12	I	I2B
2	A07	I	I2B
3	VSS	–	
4 | 9	A06 | A01	I	I2B
10	VDD	–	
11	A00	I	I2B
12	BS2	I	I2B
13	XMRD	I	I2B
14	XIOR	I	I2B
15	VSS	–	
16	XIOW	I	I2B
17	MOVR	O	O2B
18 | 25	CDA7 | CDA0	I/O	H6TF
26	VSS	–	
27	VDD	–	
28	DRQ0	O	O2B
29	XDA0	I	I2B
30 | 37	AKD7 | AKD0	I/O	H6T
38	VSS	–	
39	AKDP	I/O	H6T
40	XDAK	I	I2B
41	DREQ	O	O2B
42	CVCK	O	O2B
43	VDD	–	
44 | 49	FIO7 | FIO2	I/O	H6T
50	VSS	–	
51	FIO1	I/O	H6T
52	FIO0	I/O	
53 | 58	FA7 | FA2	I	I2B
59	SICK	I	ILB
60	VSS	–	
61	VDD	–	
62	FA1	I	I2B
63	FA0	I	
64 | 69	SX6 | SX1	O	O2B
70	EXO	O	O2B
71	ADCK	O	O2B
72	VSS	–	
73	ACKI	I	ILB
74	LDZ	I	I2B
75	MDZ	I	I2B
76	NDZ	I	I2B
77	HDZ	I	I2B
78	IDZ	I	I2B
79	VDD	–	
80	XMM	I	I2B
81	TP0	I	I2B
82	VLOK	O	O2B
83	TSMR	O	O2B
84	DLE	O	O2B
85	VSS	–	
86	DLA	O	O2B
87	DLB	O	O2B
88	DLC	O	O2B
89	DLD	O	O2B
90	XRGT	O	O2B
91	XWD	O	O2B
92	XWGT	O	O2B
93	FSFV	O	O2B
94	SYOK	I	I2C
95	BUCK	I	I2C
96	VSS	–	
97	VDD	–	
98	SEND	O	O2B
99	WGT2	O	O2B
100	RWSP	O	O2B
101	SYIM	O	O2B
102	MI7N	O	O2B
103	HEAD	I	I2C
104	SMOK	I	I2C
105	SYO4	I	I2C
106	XSI4	O	O2B
107	VSS	–	
108 | 113	D7 | D2	I/O	H6TF
114	VDD	–	
115	D1	I/O	H6TF
116	D0	I/O	
117	M17W	O	O2B
118	INT1	O	O2B
119	VSS	–	
120	INTS	I	I2C
121	FSOK	I	I2C
122 | 129	XDB7 | XDB0	O	O2B
130	VSS	–	
131	VDD	–	
132	XDBP	O	O2B
133	RDSK	I	I2C
134	GEBF	I	I2B
135	SSKG	O	O2B
136 | 138	RSB0 | RSB2	O	O2B
139 | 141	RSA0 | RSA2	O	O2B
142	VSS	–	
143	SUBR	O	O2B
144	SRAM	O	O2B
145	PROM	O	O2B
146	FROM	O	O2B
147	VDD	–	
148	XNMI	O	O2B
149	XCSM	O	O2B
150	XRSW	O	O2B
151	DDIR	O	O2B
152	STRT	O	O2B
153	MODE	O	O2B
154	VSS	–	
155	XRST	I	ILB
156	UNCF	O	O2B
157	SYOM	O	O2B
158	XMCS	O	O2B
159	XRD	I	I2B
160	XWR	I	I2B
161	SYD2	I	I2B
162	SYDX	I	I2B
163	PCK	I	ILB
164	VSS	–	
165	VDD	–	
166 | 173	A7 | A0	I	I2B
174	LGT	I	I2C
175	VCK	I	ILB
176	VSS	–	
177	VOUT	O	O2B
178	ROUT	O	O2B
179 | 182	KD7 | KD4	I/O	H6TF
183	VDD	–	
184 | 187	KD3 | KD0	I/O	H6TF
188	DAP	I	I2C
189	VSS	–	
190	BCLK	I	I2B
191 | 198	DA7 | DA0	I	I2C
199	C32M	I	ILB
200	VSS	–	
201	VDD	–	
202 | 208	A19 | A13	I	I2B

■ GGC1089 (IC338, IC339 : MAIN BOARD ASSY B) (MB814400A－70PJN)

● DRAM IC

● Block Diagram



● Pin Function

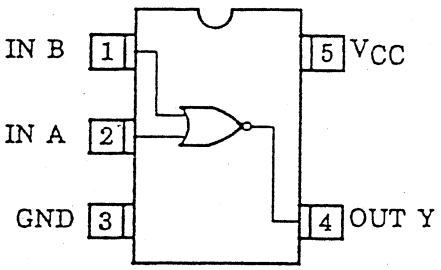
No.	Symbol	Name
1	DQ1	Data Input／Output
2	DQ2	
3	$\overline{WE}$	Write enable
4	$\overline{RAS}$	Row address strobe
5	A9	Address input
6 | 8	——	
9 | 12	A0 | A3	Address input
13	Vcc	Power supply (+5V)

No.	Symbol	Name
14 | 18	A4 | A8	Address input
19 | 21	——	
22	$\overline{OE}$	Output enable
23	$\overline{CAS}$	Column address strobe
24	DQ3	Data Input／Output
25	DQ4	
26	Vss	Power supply (0V)

■ TC7SH02FU (IC152 : MAIN BOARD ASSY B)
■ TC7S02F (IC130 : MAIN BOARD ASSY B)

● L-MOS IC

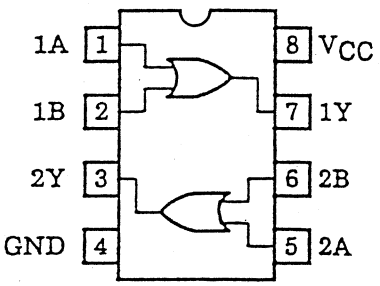
● Pin Assignment (Top View)



■ TC7W32FU (IC135, IC136, IC344 : MAIN BOARD ASSY B)

● L-MOS IC

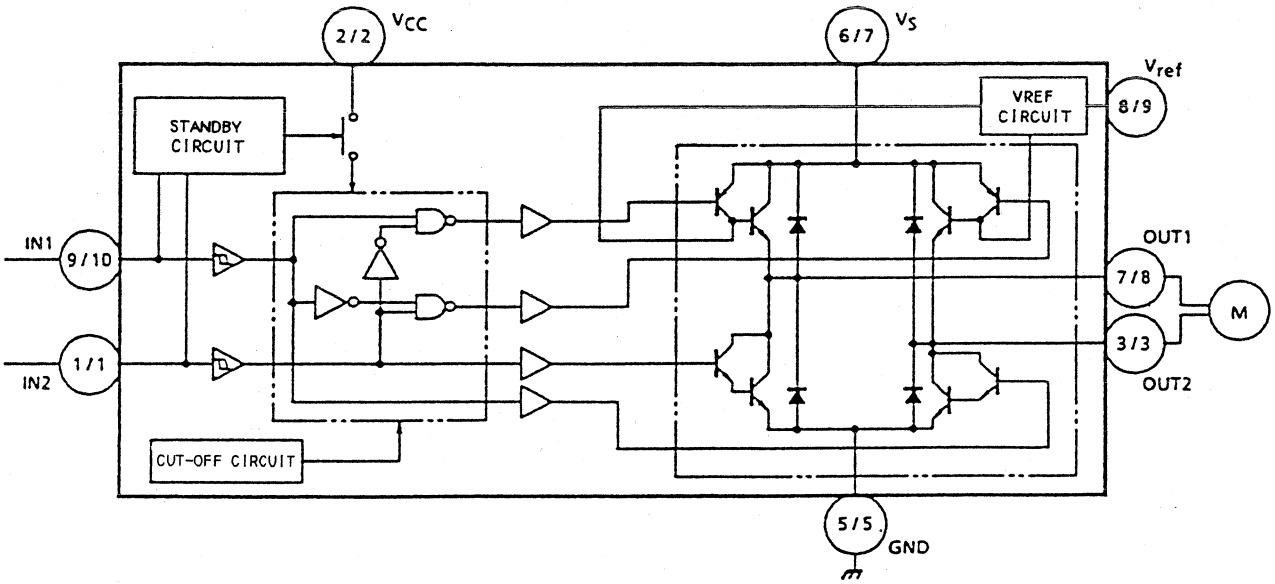
● Pin Assignment (Top View)



■ TA8409F (IC137 : MAIN BOARD ASSY B)

● Bridge Driver IC

● Block Diagram



● Pin Function

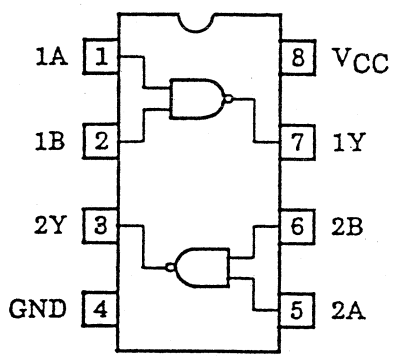
No.	Symbol	Description
1	IN2	Input terminal
2	Vcc	Logic side power supply
3	OUT2	Output terminal
4	NC	
5	GND	GND

No.	Symbol	Description
6	NC	
7	Vs	output side power supply
8	OUT1	Output terminal
9	Vref	Control power supply
10	IN1	Input terminal

■ TC7W00FU (IC111 : MAIN BOARD ASSY B)

● L-MOS IC

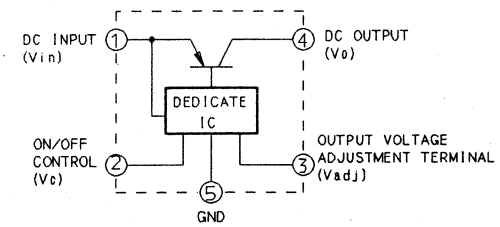
● Pin Assignment (Top View)



■ PQ20VZ51 (IC121 : MAIN BOARD ASSY B)

● Regulator IC

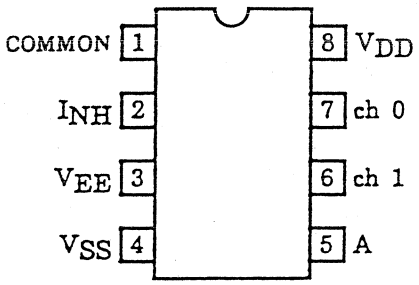
● Block Diagram



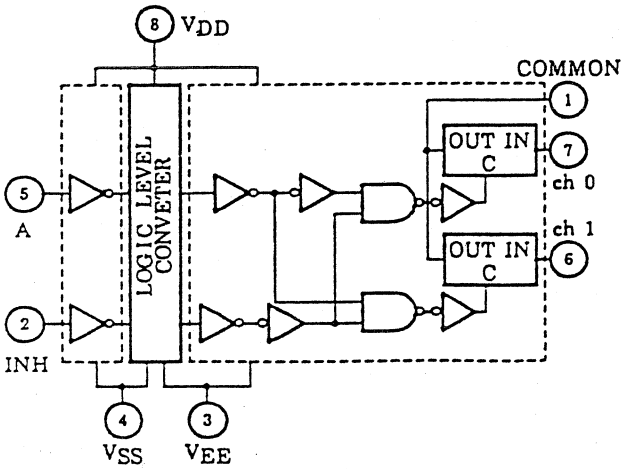
■ TC4W53FU (IC161 : MAIN BOARD ASSY B)
■ TC4W53F (IC901 : 94 SERVO BOARD ASSY)

● L-MOS IC

● Pin Assignment (Top View)



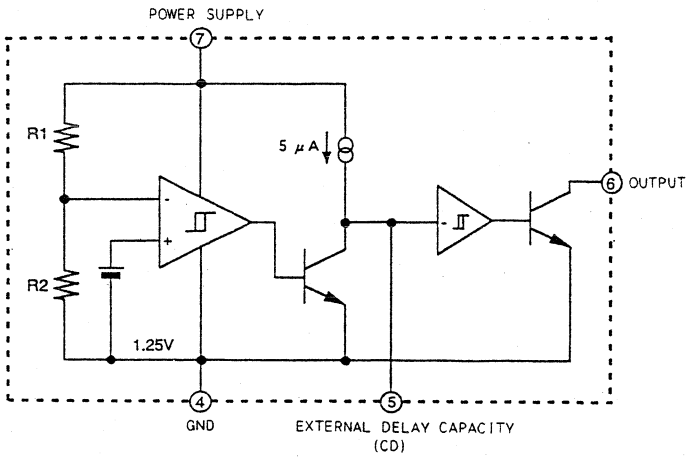
● Logic Diagram



■ M51953BFP (IC138 : MAIN BOARD ASSY B)

● Reset IC

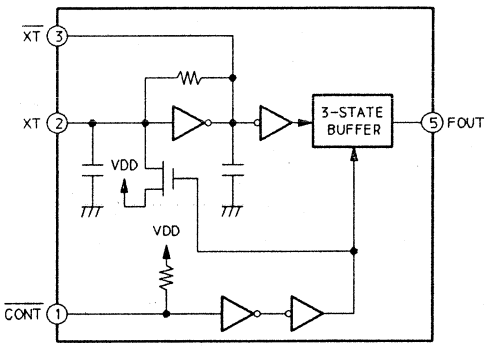
● Block Diagram



■ NJU6322KE (IC158, IC162 : MAIN BOARD ASSY B)

● X'tal Oscillation IC

● Block Diagram

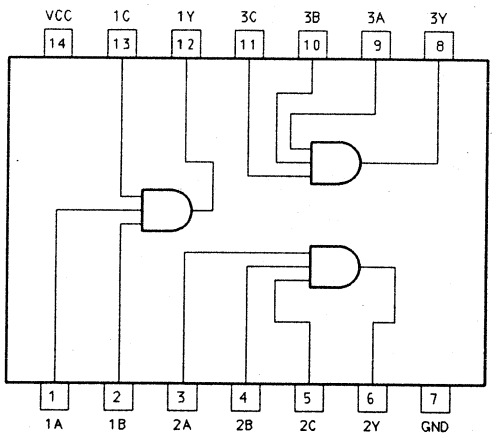


● Pin Function

No.	Pin Name	Description
1	$\overline{CONT}$	Oscillation stop and tristate output control terminal CONT: Fout H or OPEN L: Fo frequency output. Oscillation stop and output high impedance
2	XT	Connected to Crystal resonator
3	$\overline{XT}$	
4	Vss	Power supply Vss ····· GND
5	Fout	Fo frequency output
6	——	
7	——	
8	VDD	Power supply VDD ····· +5V

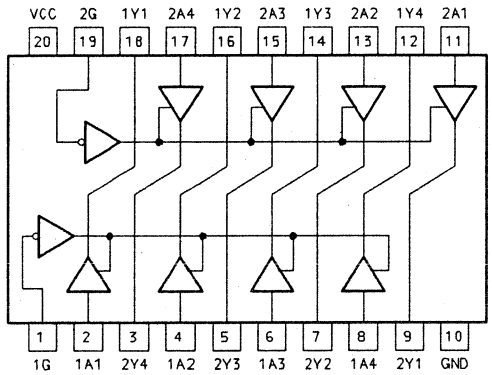
SN74ALS11ANS (IC342 : MAIN BOARD ASSY B)

- **TTL IC**
- Block Diagram



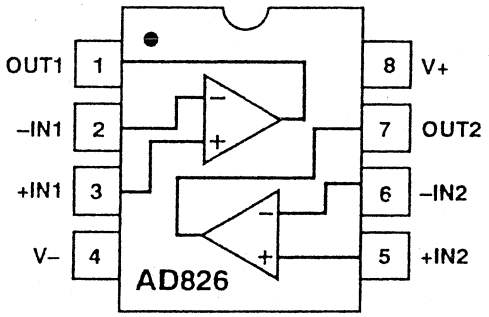
SN74ALS244BNS (IC329 : MAIN BOARD ASSY B)

- **TTL IC**
- Block Diagram



AD826AR (IC3 : PU BOARD ASSY)

- **OP-AMP IC**
- Pin Assignment (Top View)

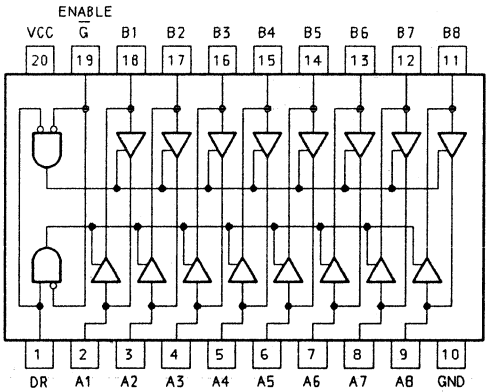


SN74ALS245ANS (IC303 : MAIN BOARD ASSY B)

- **TTL IC**

TC74HC245AF (IC345 : MAIN BOARD ASSY B)

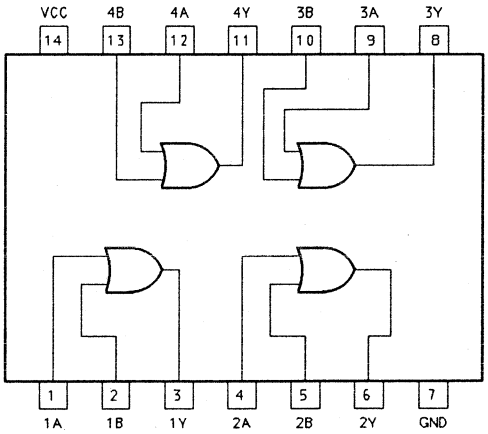
- **C-MOS IC**
- Block Diagram



SN74ALS32NS (IC341 : MAIN BOARD ASSY B)

SN74AS32NS (IC133 : MAIN BOARD ASSY B)

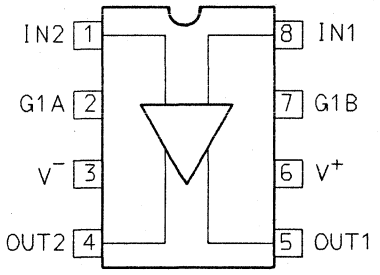
- **TTL IC**
- Block Diagram



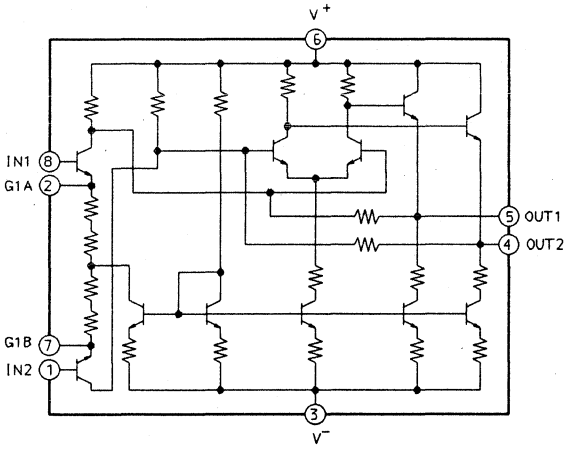
■ UPC1663G (IC1 : PU BOARD ASSY)

● Video Amp IC

● Pin Assignment (Top View)



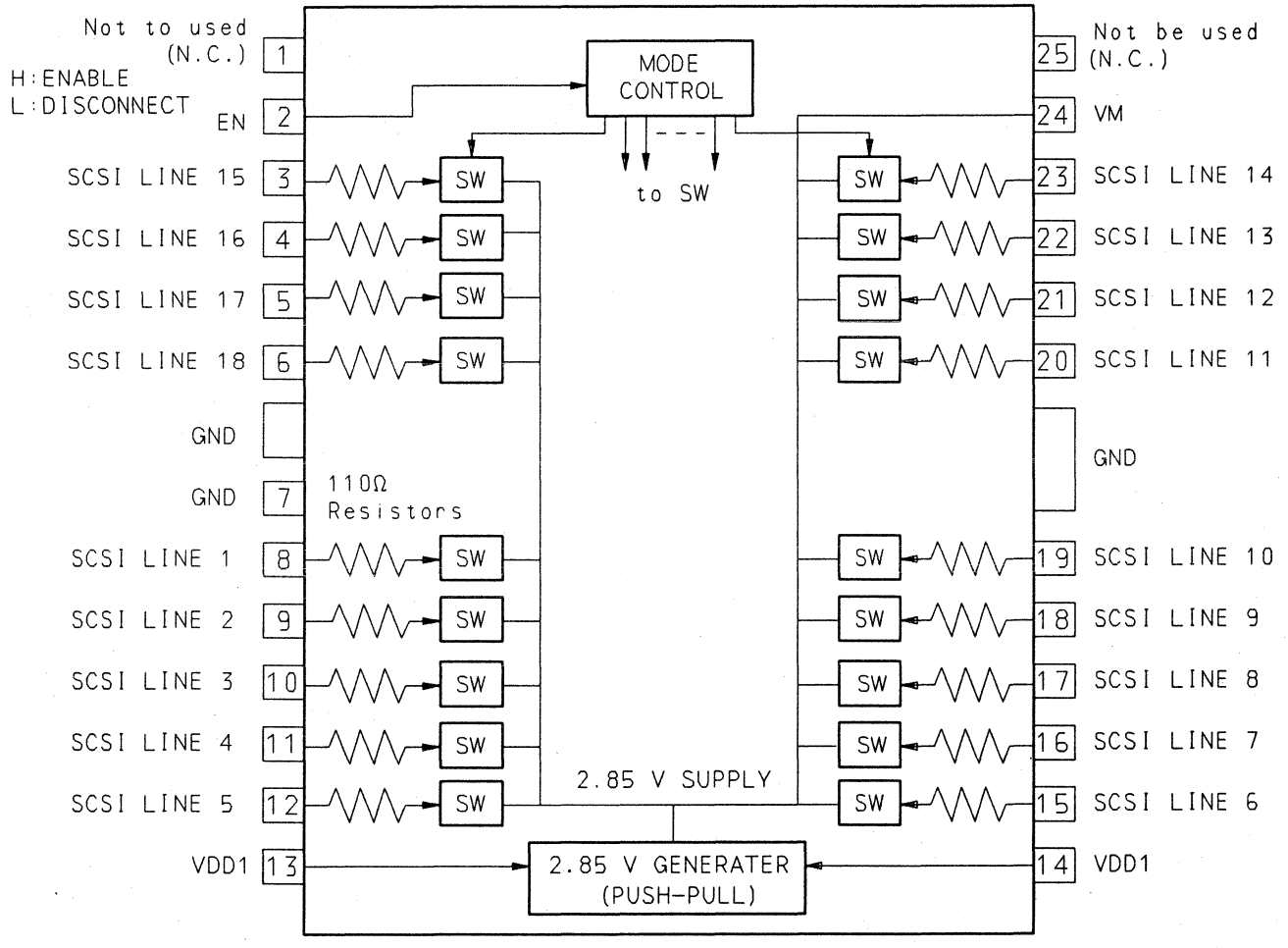
● Block Diagram



■ BH9590FP−Y (IC349 : MAIN BOARD ASSY B)

● SCSI Terminator

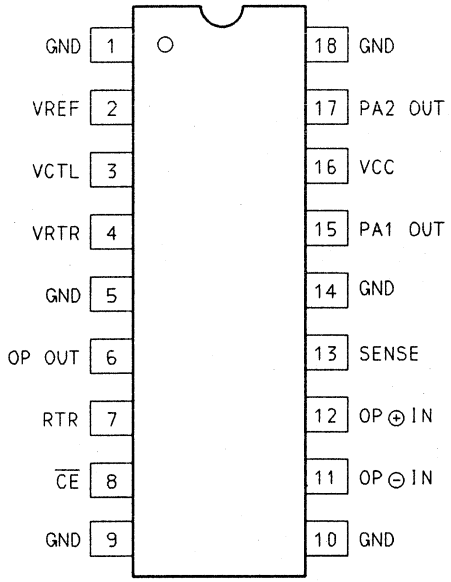
● Block Diagram



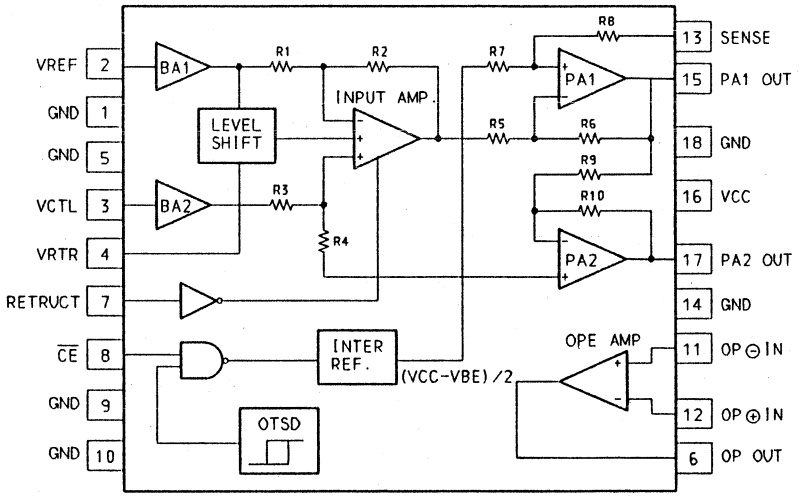
■ HA13490MP (IC411, IC412 : 94 SERVO BOARD ASSY)

● Linear Driver IC

● Pin Assignment (Top View)



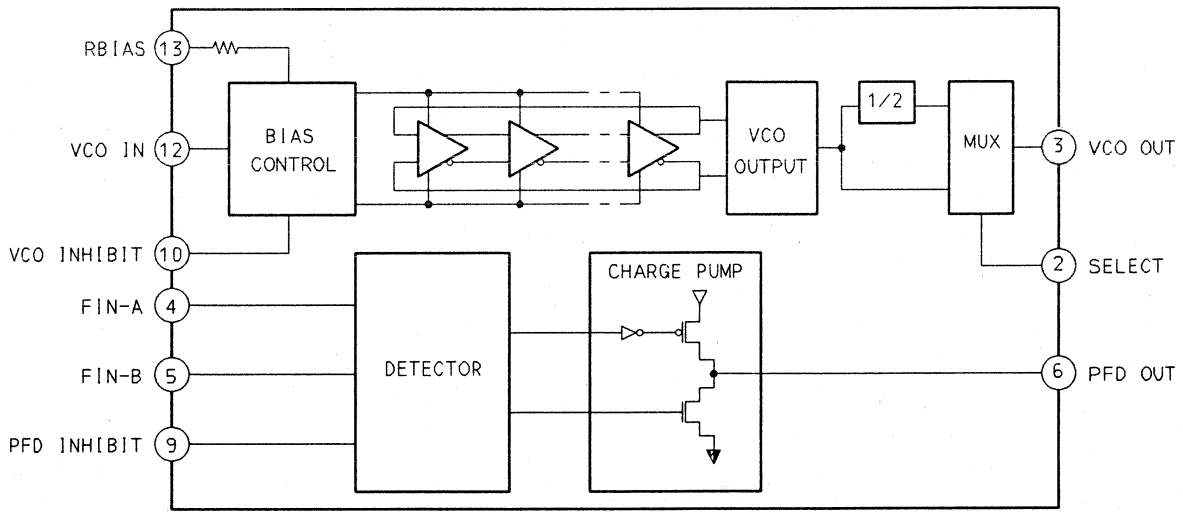
● Block Diagram



■ TLC2932IPW (IC132, IC324, IC346 : MAIN BOARD ASSY B)

● PLL IC

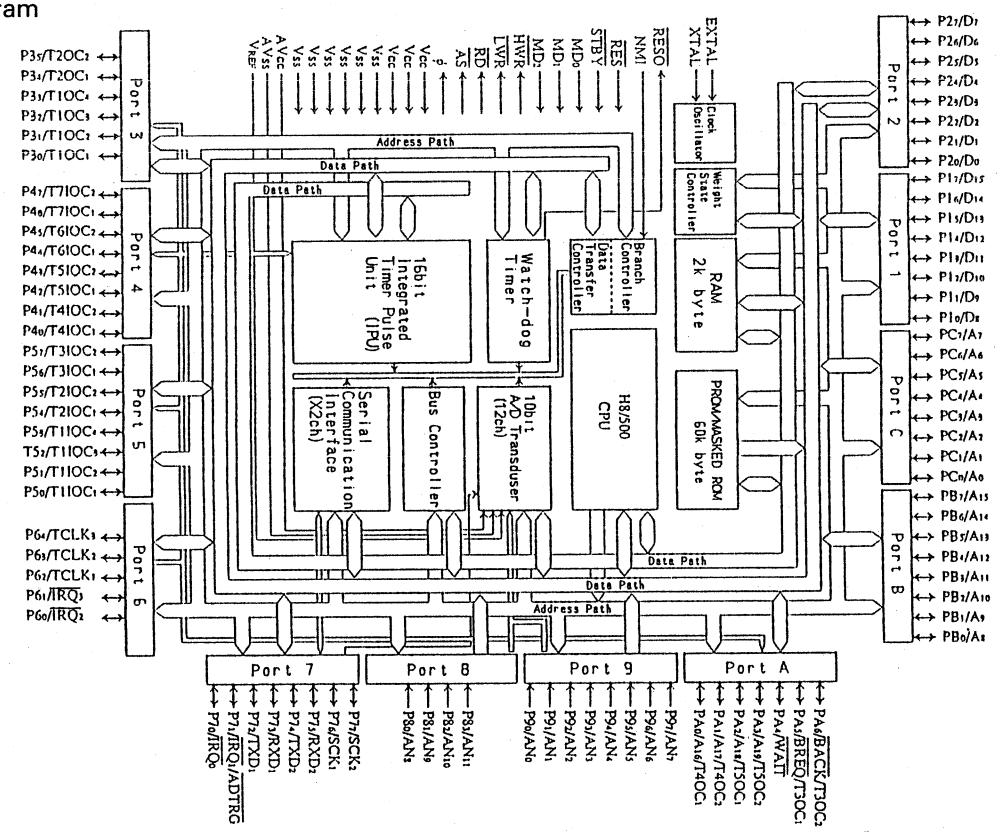
● Block Diagram



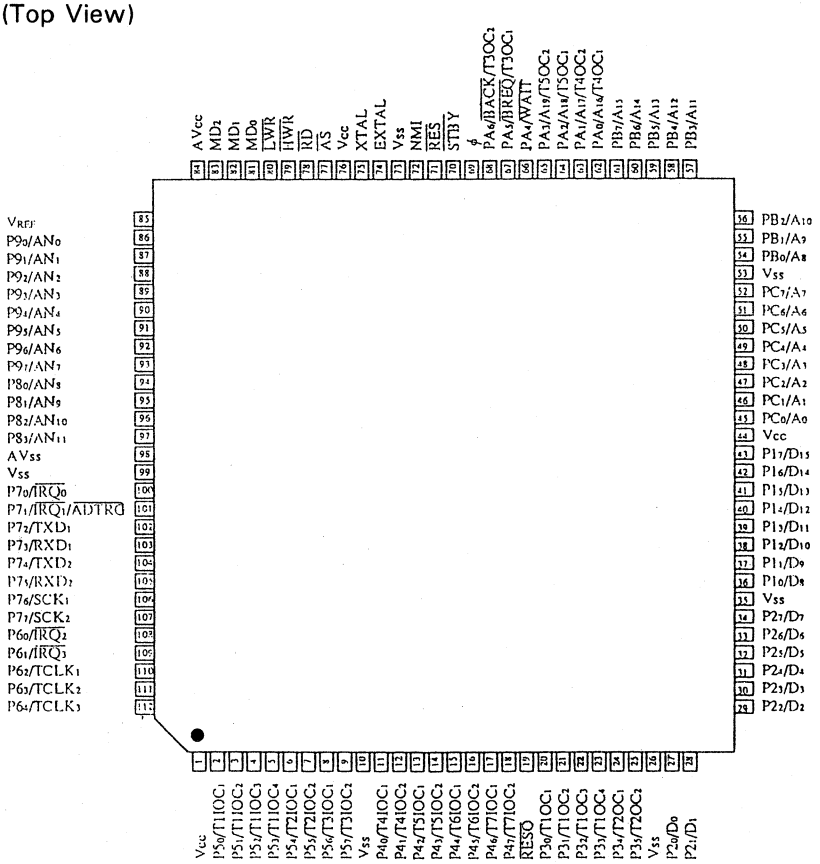
■ PD3309A9 (IC146 : MAIN BOARD ASSY B)

● Single Chip Micro-computer

● Block Diagram



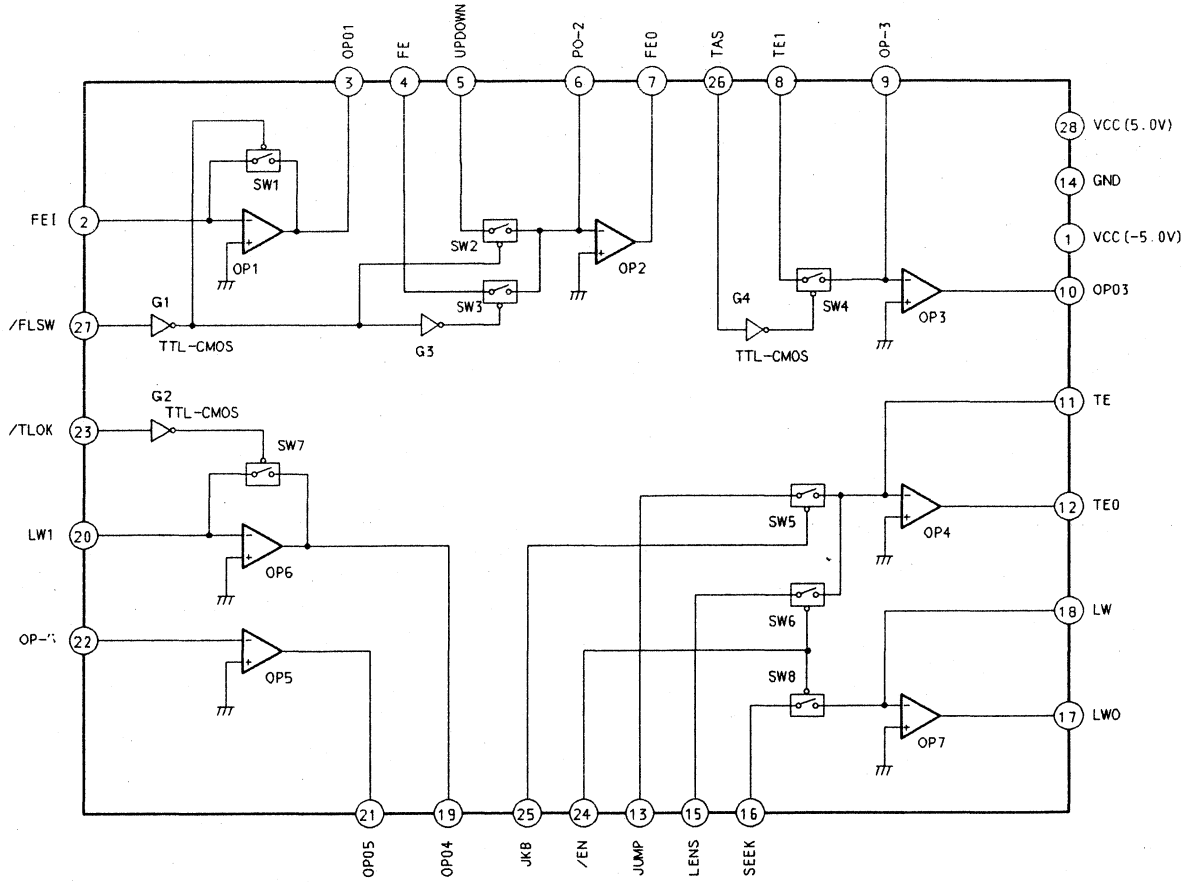
● Pin Assignment (Top View)



PA6003A (IC402 : 94 SERVO BOARD ASSY)

Servo IC

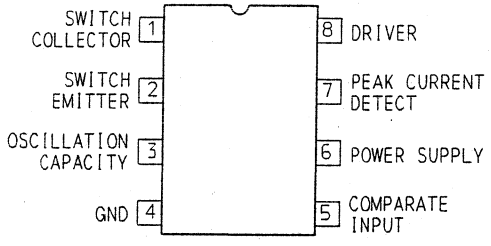
- Block Diagram



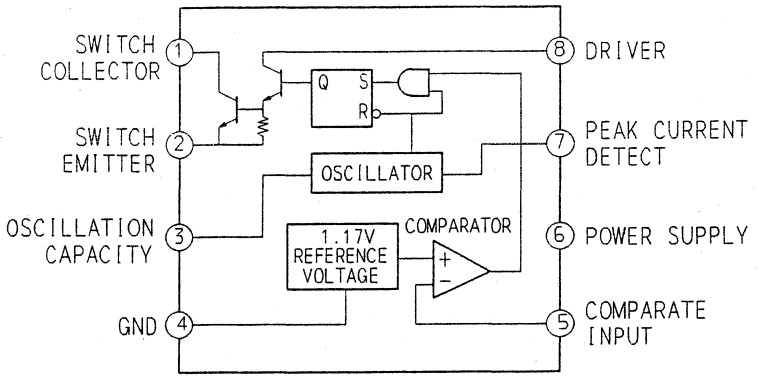
M5291FP (IC155 : MAIN BOARD ASSY B)

Switching Regulator Control IC

- Pin Assignment (Top View)

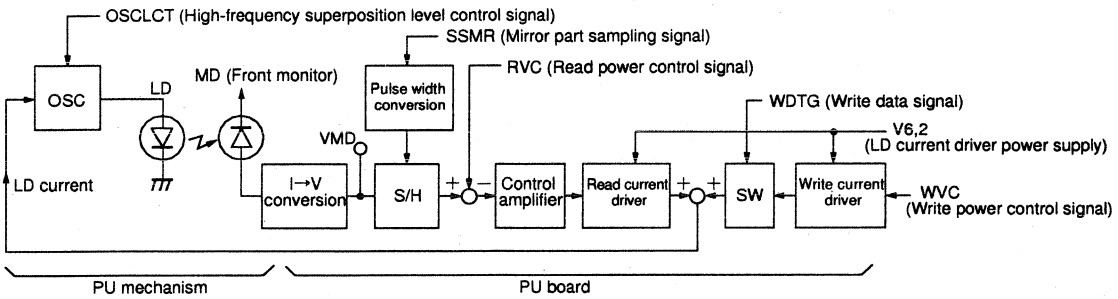


- Block Diagram



8. CIRCUIT DESCRIPTION

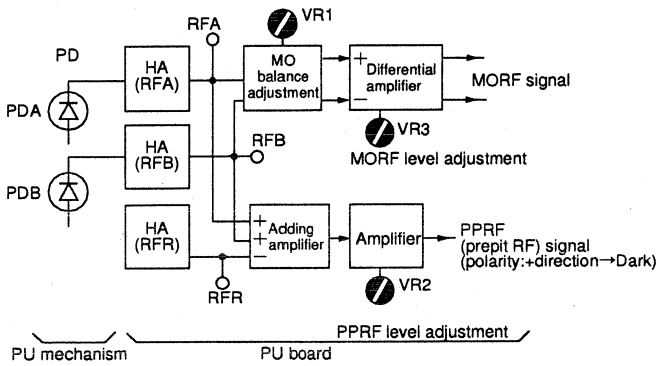
8.1 APC (LASER POWER CONTROL) CIRCUIT (PU BOARD ASSY)



- With LD ON, V6.2 is supplied and the APC circuit operates.
- A part of the light from the LD (laser diode) is received by the MD (monitor diode), I→V conversion is executed for this light, and VMD (monitor voltage proportional to the LD output power) is obtained. This is compared with the target value (RVC) via the S/H (servo hold) circuit becoming ON at the time of read power output, and the LD current is controlled so that the read power is kept constant.
- The write power is generated by using the WDTG (write data signal) to modulate (switch) a current proportional to the target value (WVC) and adding the result to the above read LD current.
- The OSC (high-frequency superposition circuit) superposes a high frequency (about 220 MHz) onto the above LD current, and this level can be changed by means of the OSCLCT (high-frequency superposition level control signal).

Note: For RVC, WVC, and OSCLCT, the voltage can be changed by the microcomputer (drive CPU), and the adjustment value is written into the EEPROM.

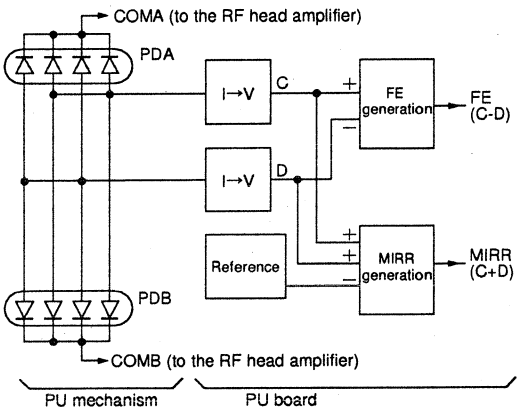
8.2 RF SIGNAL GENERATION CIRCUIT (PU BOARD ASSY)



- The current of each of the two PDs (photodetector) is subjected to I→V conversion by the HA head amplifier, and the signals RFA and RFB are obtained.
- After adjustment of the level balance for RFA and RFB, the MORF signal is obtained by differential amplification.
- The PP (prepit) RF signal is obtained by adding RFA and RFB. As the adding amplifier is a DC amplifier, RFR is used as the reference to prevent drift at the DC operation point.

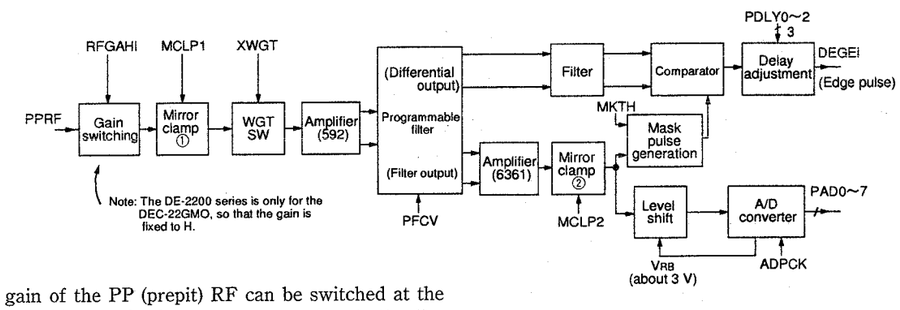
Note: MO balance, MORF level, and PPRF are adjusted by VR.

8.3 ERROR SIGNAL GENERATION CIRCUIT (PU BOARD ASSY)



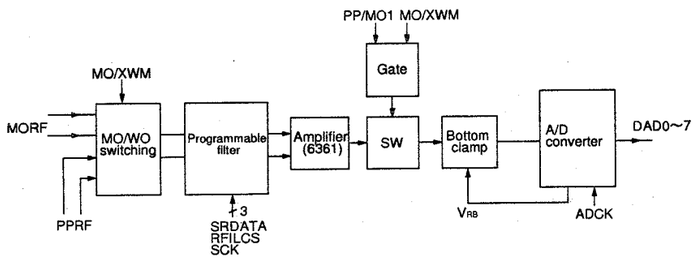
- The FE (focus error) signal is generated according to the astigmatic aberration method by a photodetector divided into four parts.
- The photodetector current is subjected to I→V conversion, the FE signal is obtained as the difference and the difference between the sum and the reference voltage for DC drift cancellation provides the MiRR (mirror) signal)
- The signal polarity is FE "+" direction →
  MiRR "+" direction → Bright

8.4 PPRF SIGNAL PROCESSING CIRCUIT, EDGE PULSE GENERATION CIRCUIT (MAIN BOARD ASSY B)



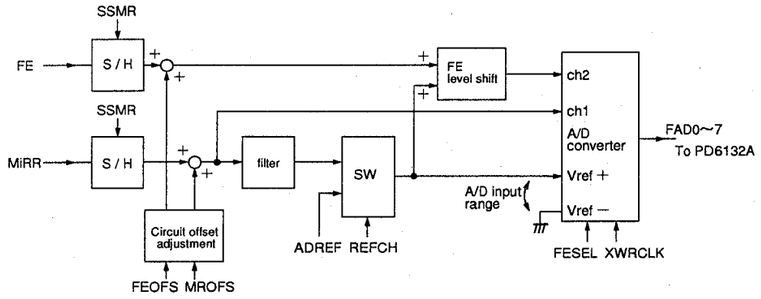
- The gain of the PP (prepit) RF can be switched at the gain switching section in two steps according to the disc type.
- Next, clamping to the ground potential is done at the mirror part of the servo byte by the mirror clamp 1 .
- Further, the WGT (write gate) SW switches the signal between erasing and writing and prevents saturation of the amplifier in the later stage by the large signal generated during erasing and writing.
- Next, the signal is amplified by the amplifier (592), and it is converted to the balance signal (positive phase, negative phase).
- Then waveform equalization is executed by the programmable filter (SSI32F8020A), and the cutoff frequency can be adjusted by changing the voltage of the PFCV from the drive CPU.
- The differential output of the programmable filter passes through a filter for noise removal, and then it is passed through the comparator to obtain the edge pulse (pulse corresponding to each pit waveform of the PPRF). Here, in order to prevent erroneous operation of the comparator because of noise etc., the comparator is switched off when the RF level drops below a specified level decided by the MKTH (mask threshold) voltage (can be adjusted from the drive CPU).
- The edge pulse passes through the delay adjustment (adjustment by bit 3 of PDLY0 to 2) and enters the PCK (servo sync clock) generation part.
- The filter output from the programmable filter passes through the amplifier (6361), and after the mirror part again is clamped to the GND potential by the mirror clamp 2 , the DC level of the signal is shifted in the level shift circuit so that it falls into the input range [VRB (3 V) to VCC (5 V)] of the A/D converter.
- The level-shifted PPRF signal is subjected to A/D conversion with the ADPCK timing by the A/D converter (8 bit/25 MHz) and is sent to the PD6132A (servo LSI).

8.5 DATA RF SIGNAL PROCESSING CIRCUIT (MAIN BOARD ASSY B)



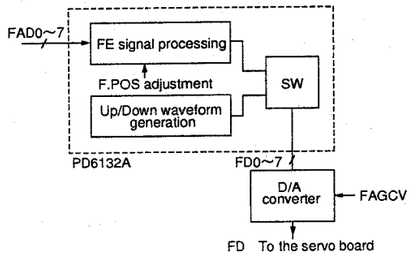
- The MO/WO switching part uses the MO/XWM signal for switching between MORF and PPRF (switching to this side is done for reading of the SFP area or reading of data from a WORM disc. As the DE−2200 series is only for MO, this is only for reading the SFP area.)
- The programmable filter has a three-line serial interface and can change the cutoff frequency from the drive CPU and the boost amount, and optimal waveform equalization is executed according to the disc zone and the disc radius position.
- After waveform equalization, the data RF signal passes through the amplifier (6361) and enters into the switch SW. This switch is set up so that it becomes OFF at the servo byte part, and in the bottom clamp circuit of the next stage, clamping is done by the servo byte part (with an MO disc, the potential is indefinite), and changing of the potential of the data part is prevented.
- The bottom clamp is used to bring the data RF signal into the input range (VRB = 3 V to VCC = 5 V) of the A/D converter. (The bottom is clamped so that it comes to about 250 mV above VRB.)
- A/D conversion is executed by the A/D converter (8 bit/40 MHz) with the ADCK timing, and the signal is sent to the PD6133A (read/write LSI).

8.6 FE, MIRR SIGNAL PROCESSING (MAIN BOARD ASSY B)



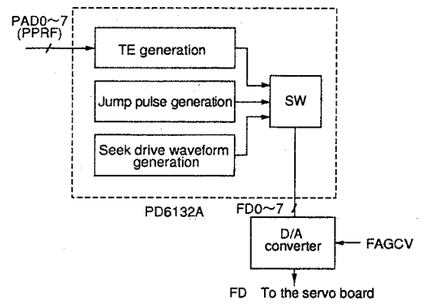
- First, the SSMR executes S/H (sample hold) for FE and MiRR signal, and the circuit system offset is removed by the circuit offset adjustment part. (The drive CPU executes automatic adjustment.)
- The FE signal is shifted by the level shift circuit so that it deflects around the center point of the input range (Vref− to Vref+) of the A/D converter (4 channel input, however, only two channels are used here), and then it is given as input to the A/D converter.
- At this time, the MiRR signal selected by the REFCH signal at the switch part is given as input to Vref+, so that the A/D-converted FE is normalized by MiRR. In other words, a constant gain is maintained for FE independent of the amount of return light.
- On the other hand, the MiRR signal also is given as input to the A/D converter, but at this time, a fixed voltage (ADREF set by the drive CPU) is given as input to Vref+ by SW.
- After A/D conversion, the FE and MiRR signals are sent to PD6132A (servo LSI).

8.7 FD GENERATION (MAIN BOARD ASSY B)



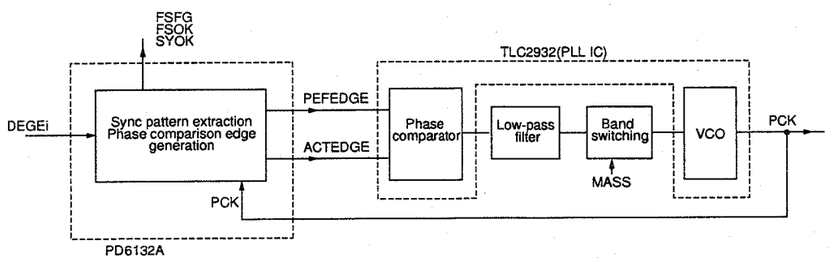
- The FD signal is the drive signal for the focus servo system, and it is obtained by D/A conversion of the data signals FD0 to 7.
- The FD signal is multiplexed, and when the control signal for up/down for the objective at the time of in-focus closes the focus, the FE signal is put out.
- The up/down waveform is a triangular wave with rounding processing having been executed for the peak part to prevent loss of focus by vibrations of the objective because of rapid changes at the peak part.
- F. POS (focus position) adjustment is executed for the FE signal, but this adjustment is executed automatically inside PD6132A so that the PPRF level becomes a maximum.
- The level of the FD signal can be changed by controlling the reference for the D/A converter by FAGCV from the drive CPU. This is used to adjust the focus servo gain.

8.8 TD GENERATION (MAIN BOARD ASSY B)



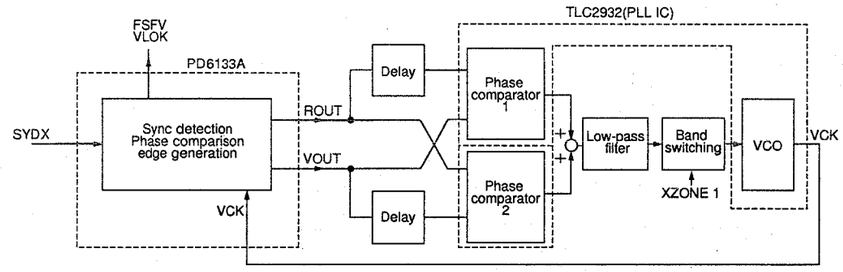
- The TD signal is the drive signal for the carriage servos (tracking servo and linear motor servo), and it is obtained by D/A conversion of the data signals TD0 to 7 of PD6132A.
- The TD signal is multiplexed, and during tracing in tracking open or tracking close condition, the TE (tracking error) signal is put out, while the kick/brake jump pulse is put out at the time of jump and the signal driving the linear motor by means of the profile servo is put out at the time of seek.
- The TE signal is obtained by comparing the PPRF wobble pit level and reversing the polarity for odd/even tracks. (In case of MASS format) This is generated by digital calculations inside the PD6132A.
- The level of the TD signal can be changed by controlling the D/A converter reference with TAGCV from the drive CPU.This is used for adjustment of the tracking servo gain and the profile servo gain.

8.9 PCK (SERVO SYNC CLOCK) GENERATION PLL CIRCUIT (MAIN BOARD ASSY B)



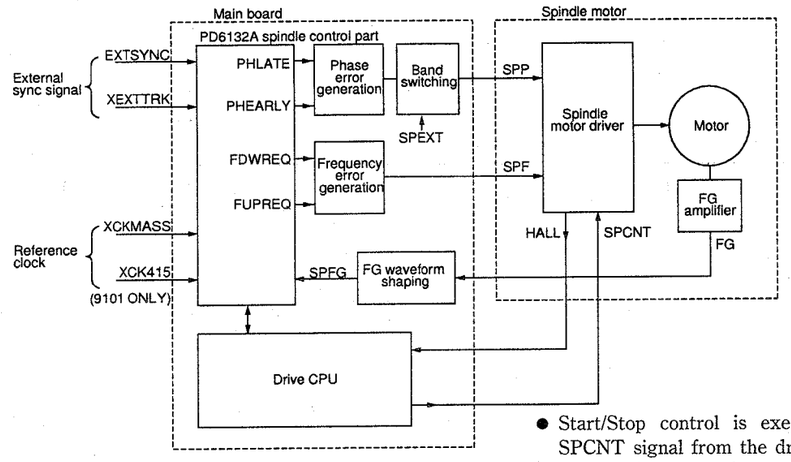
- DEGEi (edge pulse generated from PPRF) is given as input, the sync pattern is extracted, and the edge for phase comparison is generated.
- Phase comparison is executed for these edges (REFEDGE and ACTEDGE), input is made to VCO (voltage control oscillator) via the low-pass filter, and a PLL (phase-locked loop) is formed.
- Band switching is used for band switching for MASS discs and 4/15 discs.
- This PLL generates the PCK (servo sync clock), and this is used as the basis for the generation of various timing signals.
- FSFG, FSOK, and SYOK are put out from PD6132A as flags indicating the sync status.

8.10 VCK (READ/WRITE SYNC CLOCK) GENERATION PLL CIRCUIT (MAIN BOARD ASSY B)



- The SYDX (clock edge) signal obtained from PD6132A is given as input, sync detection is executed, and the edges (ROUT and VOUT) for phase comparison are generated.
- These are given as input to two phase comparators, but at this time, one signal is given as input after being delayed by a delay circuit.The outputs of the two phase comparators are added and become the phase comparison result. This is done to shift the phase comparison operation point and avoid the influence of the insensitive band of the phase comparator near the zero point of the phase difference.
- The phase comparison is given as input to the VCO after passing through the low-pass filter, and a PLL is formed.
- Band switching is executed by XZONE1 according to the disc zone.
- VCK is generated from VCO, and the read/write clock timing is generated.
- FSFV and VLOK are put out from PD6133A as flags indicating the sync status.

8.11 SPINDLE MOTOR CONTROL (MAIN BOARD ASSY B, SPINDLE MOTOR)

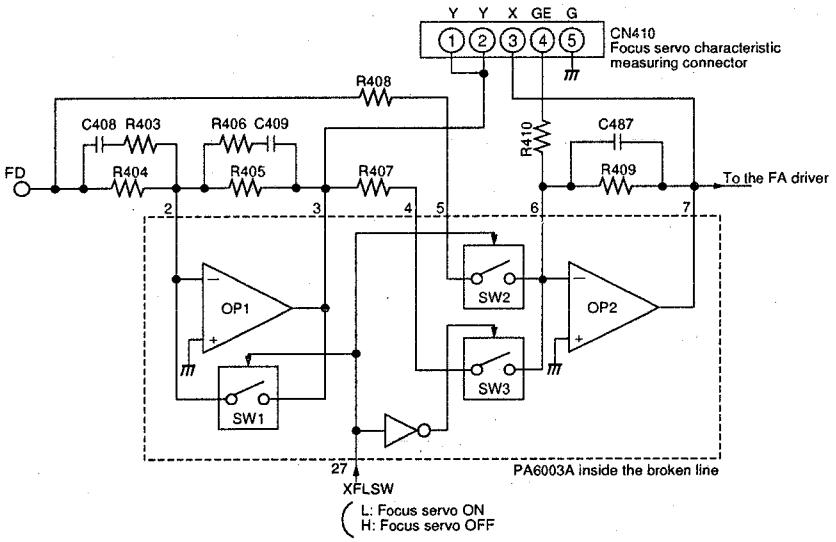


- Speed control for the spindle motor by itself is not possible. Operation is made in combination with the control part of the main board.
- PLL control is executed for the motor, a pulse signal is generated by PD6132A according to the pitch of the frequency or the phase advance or delay, this is used to produce the frequency error signal and the phase error signal, input is made to the spindle motor, and the motor runs. For monitoring the speed, waveform shaping is executed for the FG signal of the motor, and the SPFG signal is fed back.
- Start/Stop control is executed by the SPCNT signal from the drive CPU, and the rotation status is monitored via the HALL signal.
- Normally, rotation at constant speed is executed on the basis of the reference clock, but the speeds or the rotation angles of several drives can be synchronized by input of an external sync signal.

8.12 SERVO CIRCUIT (94 SERVO BOARD ASSY)

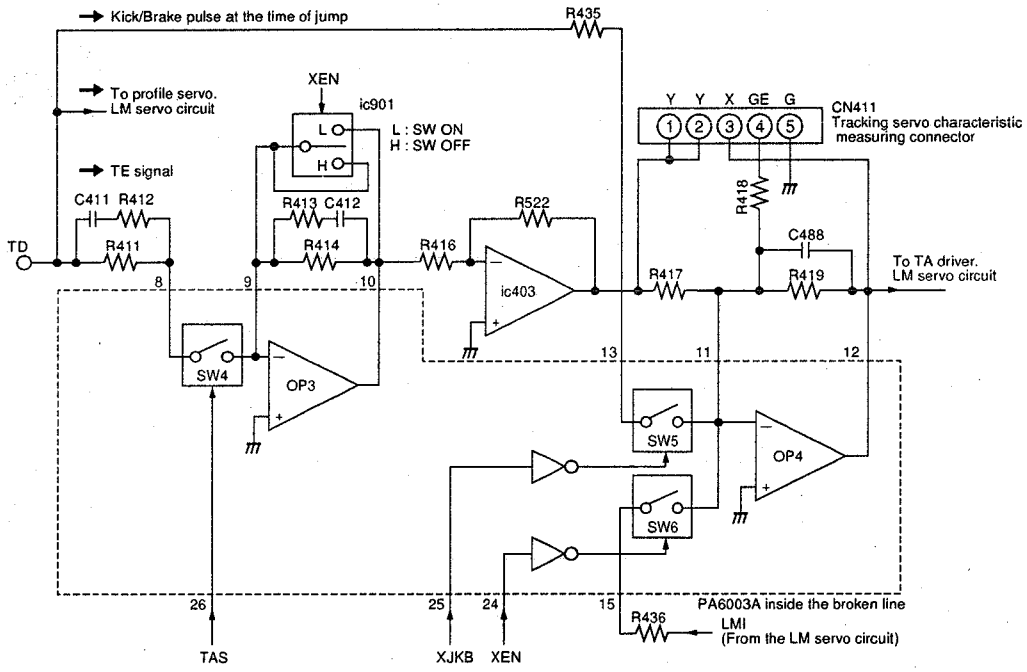
- This is the part executing phase compensation for focus, tracking, and linear motor servo, servo ON/OFF control, etc., and it is composed with PA6003A in the center.
- The circuit diagram including the internal circuits of the PA6003A can be expanded as follows.

1. Focus Servo Circuit



- This is composed of a two-stage amplifier, where the first stage serves as an equalizer for phase advance compensation and an integrating amplifier, while the second stage serves as an amplifier for measuring the servo characteristics and as a low-pass filter for removal of high band noise.
- At the time of focus servo OFF, SW1 becomes ON, SW2 becomes ON, and SW3 becomes OFF, the FD signal is applied to the amplifier OP2 of the second stage, and the up/down waveform at the time of in-focus is transmitted to the FA driver.
- At the time of focus servo ON, SW1 and SW2 become OFF, SW3 becomes ON, the FD signal passes through the amplifier OP1 of the first stage and is applied to the amplifier of the second stage, where the focus servo loop is formed.
- When a servo analyzer is connected to the servo characteristic measuring connector, an external disturbance is applied to GE, and Y/X is measured, the open loop servo characteristic is obtained. However, the amplifier characteristic of the second stage is not included.

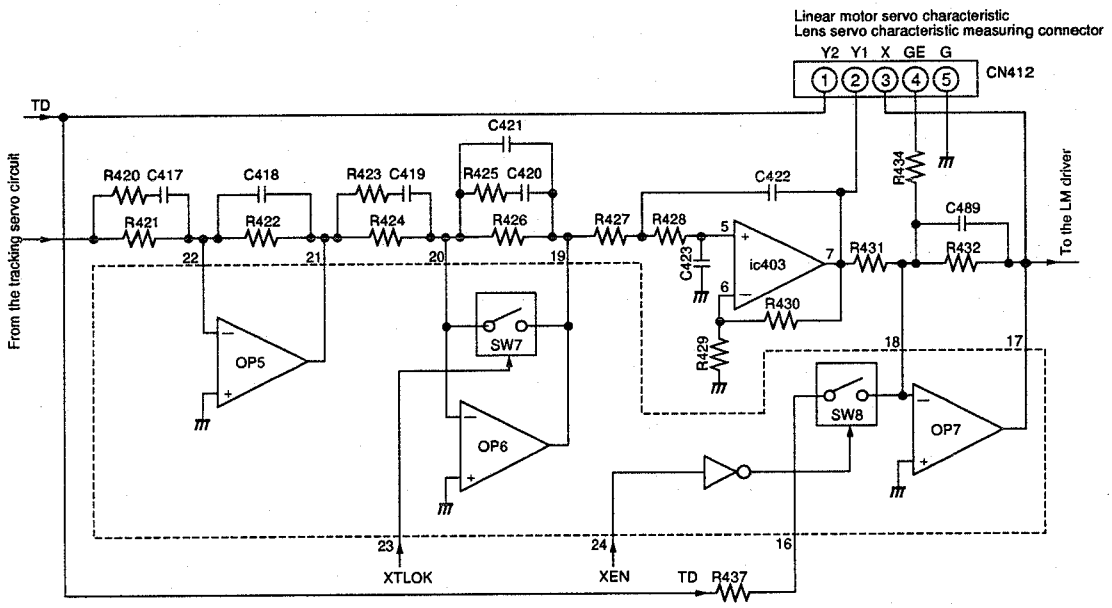
2. Tracking Servo Circuit



Notes:
TAS: "H" with tracking servo ON, "L" with servo OFF and during jump or seek.
XJKB: "L" during jump, otherwise "H".
XEN: "L" during seek, otherwise "H".

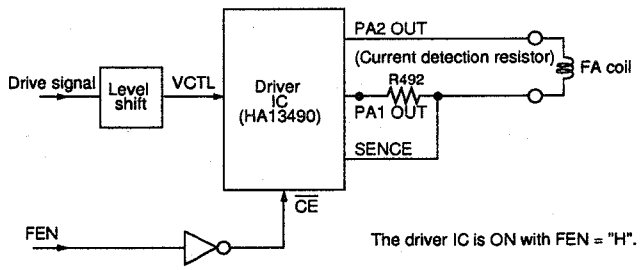
- This is composed of a three-stage inversion amplifier. The first stage serves as an equalizer for phase advance compensation and an integrating amplifier, the second stage serves as a flat amplifier, and the third stage serves as an amplifier for servo characteristic measuring and a low-pass filter for removal of high range noise.
- At the time of tracking servo OFF, SW4 becomes OFF, SW5 and SW6 become OFF, and TA is not driven.
- At the time of tracking servo ON, SW4 becomes ON, IC901 becomes OFF, the TE signal is given as input from TD, and the servo loop is formed.
- At the time of jump, SW4 becomes OFF, SW5 becomes ON, the kick/brake pulse is given as input from TD, and it drives TA through OP4.
- At the time of seek, SW4 becomes OFF, IC901 becomes ON, the linear motor drive signal for the profile servo is generated for TD, and seeking is executed. As the DC gain of the integration amplifier by OP3 is high and a large DC offset is generated as the OP3 output at the time of seek, IC901 is installed to remove this. Further, SW6 becomes ON and TA is driven according to the LMI (linear motor current). This is the lens deflection compensation for prevention of deflection by the inertia of the objective at the time of linear motor acceleration/deceleration.
- When a servo analyzer is connected to the servo characteristic measuring connector, an external disturbance is applied to GE, and Y/X is measured, the open loop servo characteristic is obtained. However, the OP4 amplifier characteristic is not included.

3. Linear Motor Servo Circuit



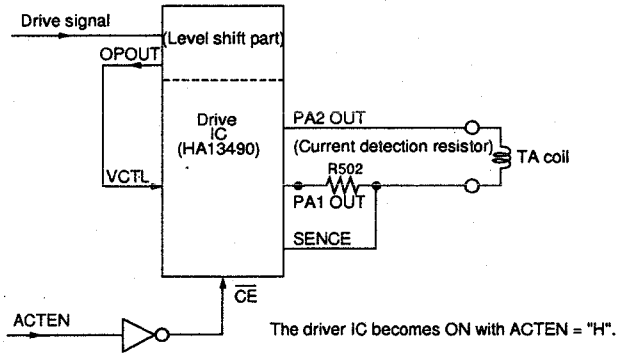
- The tracking servo and the linear motor servo form a dual servo loop, and the linear motor extracts the low-frequency component of the tracking drive signal and applies the servo.
- The circuit is composed of a four-stage amplifier. The first stage (OP5) serves for phase advance compensation and as a low-pass filter, the second stage (OP6) serves for the other phase advance compensation and as an integrating amplifier, the third stage serves as a secondary low-pass filter for removal of the high band component, and the fourth stage (OP7) serves as a servo characteristic measuring amplifier and as a low-pass filter.
- At the time of linear motor servo OFF, SW7 becomes ON, SW8 becomes OFF, and the linear motor is not driven at all.
- At the time of linear motor servo ON, SW7 becomes OFF, and the linear motor servo loop is formed.
- At the time of seek, SW7 and SW8 become ON, and the profile servo linear motor drive signal generated by TD is transmitted to the LM driver.
  Further, at the time of start-up, the drive signal from TD also is impressed to push the carriage to the inner circumference, and it is transmitted to the LM driver.
- When a servo analyzer is connected to the servo characteristic measuring connector, an external disturbance is applied to GE, and Y1/X is measured, the open loop servo characteristic of the linear motor is obtained. When the lens servo is switched on and Y2/X is measured, the lens servo characteristic is obtained. However, the OP amplifier characteristic is not included.

8.13 FA (FOCUS ACTUATOR) DRIVE CIRCUIT (94 SERVO BOARD ASSY)



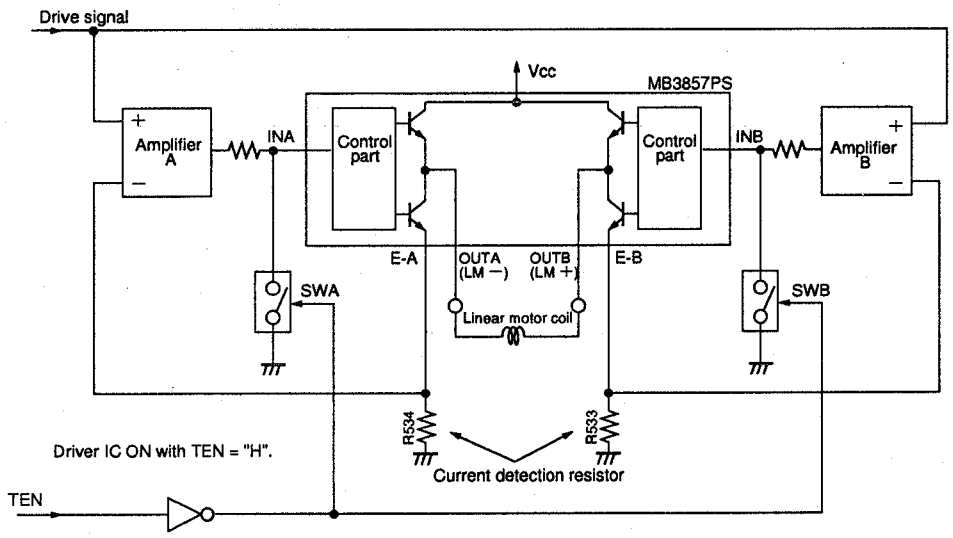
- The FA drive circuit is a current driver, and a current corresponding to the drive signal input flows to FA.
- As the driver IC is a single power supply, the drive signal is entered with a level shift to 1/2 of the potential of the driver IC power supply (Vcc = 5 V). The level shift part also serves as a low-pass filter for removal of the high-range component.
- The driver IC is switched on and off by the FEN signal.

8.14 TA (TRACKING ACTUATOR) DRIVE CIRCUIT (94 SERVO BOARD ASSY)

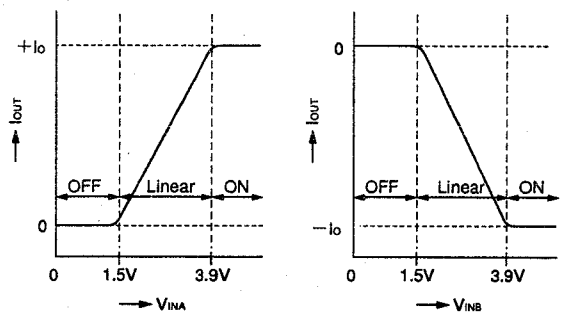


- The composition is the same as that of the FA drive circuit, where the difference is that the level shift part uses an operation amplifier with built-in HA13490. The reason for this is that the power supply voltage of the FA driver IC is +5 V and the "+" part of the amplitude of the output of the built-in operational amplifier can not be secured, so that level shifting is done by external resistance allotment, while the TA driver IC is a +12 V power supply, so that the problem of the output amplitude does not occur.

8.15 LM (LINEAR MOTOR) DRIVE CIRCUIT (94 SERVO BOARD ASSY)

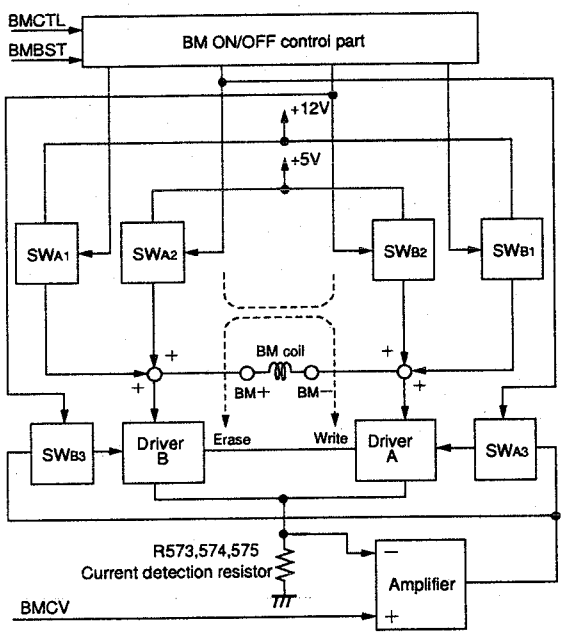


I/O characteristic of MB3857PS



- The driver IC MB3857PS basically is a bridge driver, but linear operation of VINA and VINB is obtained in the range from 1.5 V to 3.9 V. This characteristic is used to compare the drive signal input and the voltage at the current detection resistor by amplifier A and amplifier B and to form a current driver controlling VINA and VINB.
- When VINA and VINB both are kept to 1.5 V or less, the output becomes OFF (open), so that the driver IC becomes OFF when SWA and SWB are switched on by the TEN signal (linear motor driver ON/OFF signal) and VINA and VINB both become 0 V.

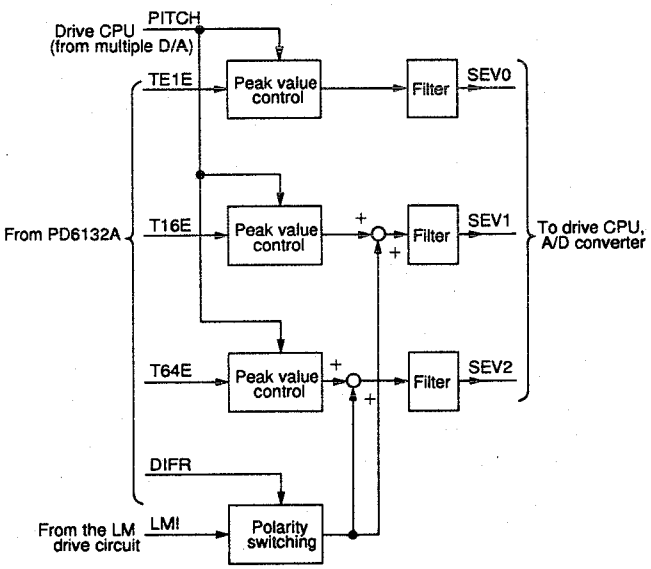
8.16 BM (BIAS MAGNET) DRIVE CIRCUIT (94 SERVO BOARD ASSY)



- Basically, this is a bridge driver. SW is driven by the BM ON/OFF control part, the polarity of the current flowing to the BM coil is switched according to erase/write, and the current value is controlled by current detection resistor, amplifier, and driver part.

- The BM CTL signal is put out by the drive CPU as a three-state control signal with 0 V for write, 2.5 V for OFF, and 5 V for erase.
- The BM BST signal is a ghost signal for acceleration of the rise of the BM current when BM is switched on, and it is a pulse signal put out from the drive CPU.
- BMCV is the BM current control voltage put out from the drive CPU via multiple D/A converters.
- For example, operation is executed as follows at the time of writing.
  ① BMCTL becomes 0 V and SWA2 and SWA3 become ON.
  ② BMCV becomes the specified voltage, this is compared with the voltage at the current detection resistor, and current flows to the driver A.
  ③ As the BM coil is an inductance load, the current flowing there increases with a specified time constant until the current value decided by BMCV is reached. In order to shorten this time, SWA1 is switched on by the BMBST signal for a fixed time after BM ON, and voltage from the +12 V power supply is impressed. Afterwards, SWA1 is switched off, and current from the +5 V power supply is supplied via SWA2.
- In other words, +12 V power is supplied only during the rise time, while normally +5 V power is used, thus reducing the power consumption of the circuit and suppressing the heat generation.

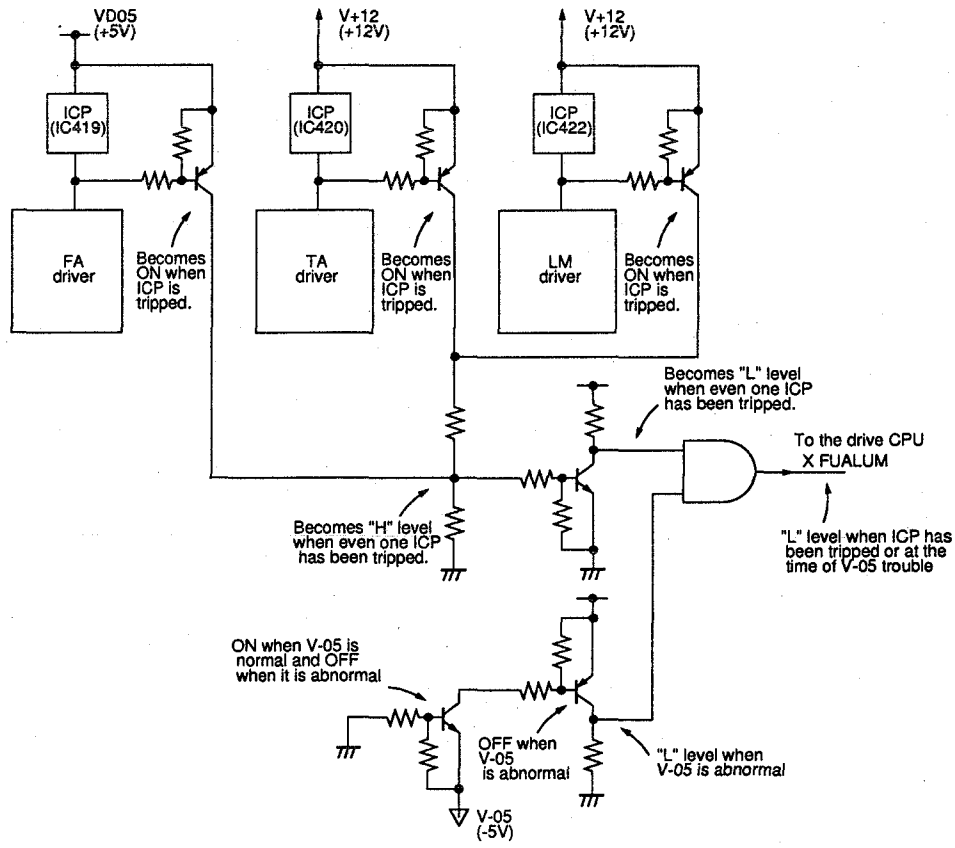
8.17 CARRIAGE SPEED DETECTION CIRCUIT (94 SERVO BOARD ASSY)



- The track count pulse generated by PD6132A is used as the basis for detection of the carriage feedrate at the time of seek etc.
- There are three types of track count pulses: TE1E (1 track count), T16E (16 track count), and T64E (64 track count) *1.
- As the track pitch of a MASS format disc differs according to the radius position (variable track pitch), the peak value of the track count pulse is changed by the PITCH signal to compensate for this.
- When this pulse is passed through the low-pass filter, the speed detection signals SEV0, SEV1, and SEV2 are obtained, and LMI (linear motor current) with the polarity switched according to the feed direction is added to SEV1 and SEV2 to compensate for speed detection errors caused by a coarse pulse interval.

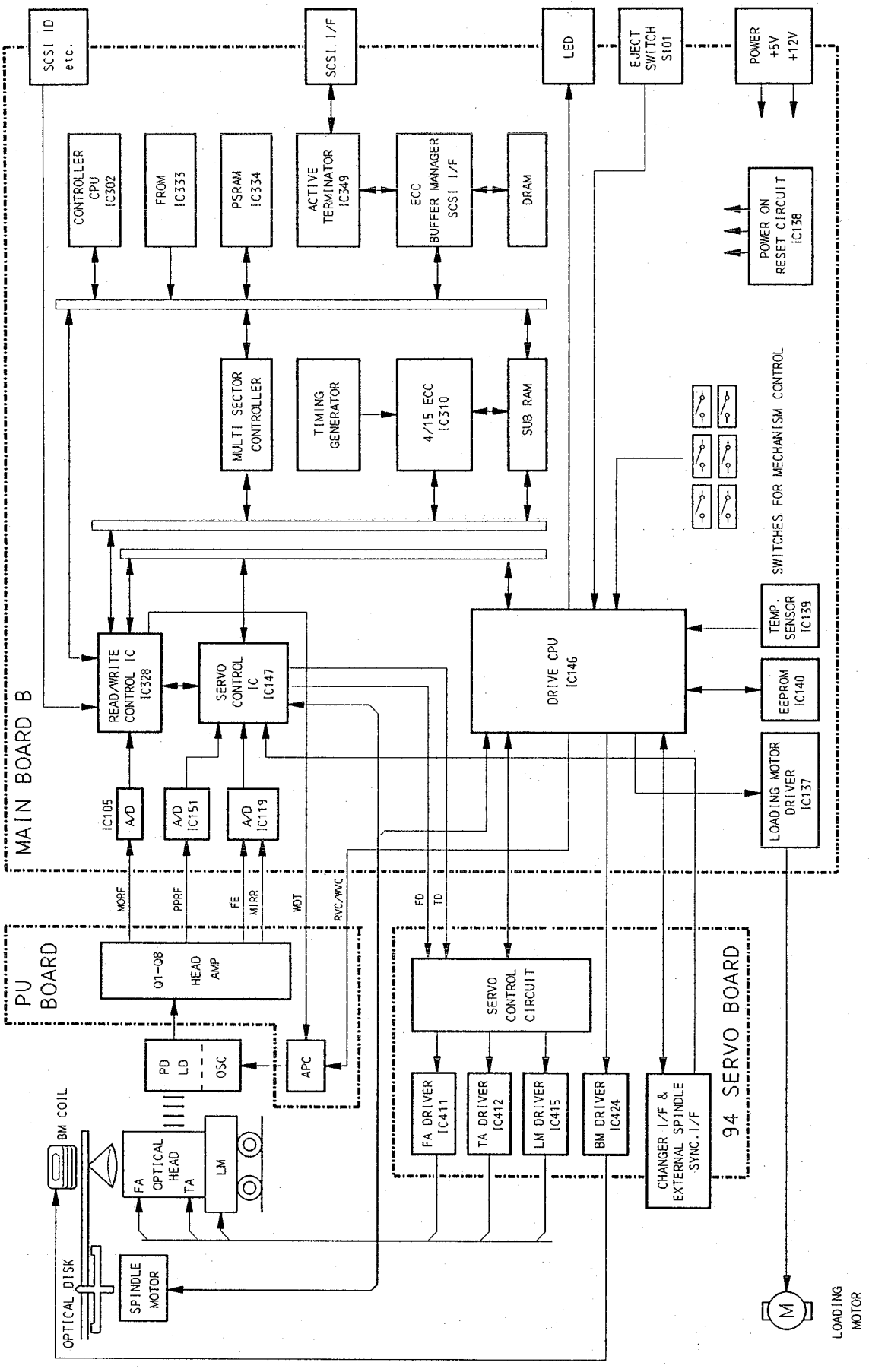
*Note *1: In the case of the MASS format, 64 track count pulses exist, but in the case of the 4/15 format (only the DE−9101 series), only the 1 track count and the 16 track count are used, so that the pulse width of T64E is reduced to the same timing as T16E and SEV2 becomes 1/4 of the level of SEV1.*

8.18 ICP TRIP, −5 V POWER SUPPLY TRIP DETECTION CIRCUIT (94 SERVO BOARD ASSY)

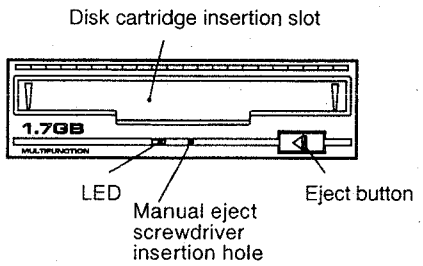


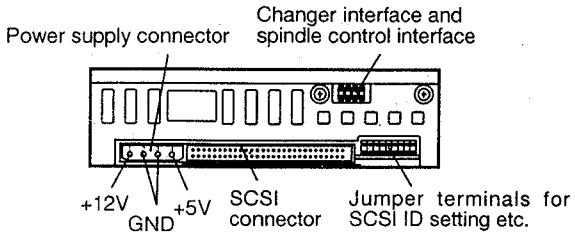
- An ICP (IC protector) is connected to the power supply of each driver IC, and if the ICP should be tripped, the servo system naturally will not operate. However, in that condition the drive will repeat return operation, so that depending on the case, the trouble may be expanded, which is not desirable.
- Also, as V−05 (−5 V power supply) is produced by the DC/DC converter inside the drive, only the −5 V side of the ±5 V power supply for the servo system operation amplifier etc. will be lost when the −5 V power supply is lost, a large DC offset will be caused for the input of each driver circuit, and an overcurrent will flow for actuators and linear motor.
- Trouble as described above is detected by the drive CPU, and trouble expansion can be prevented by switching off the ON/OFF control signal of the driver IC.
- The detection circuit has the composition shown above, and at the time of trouble, XFUALM becomes "L" level.

9. BLOCK DIAGRAM



10. PANEL FACILITIES





11. SPECIFICATIONS

- Interface : SCSI-2*1
- Rotational speed : 2700rpm, ZCAV (when a DEC-17GMO or DC-17GWO is used)
  2400rpm, CAV (when a DEC-702 or DC-502A is used)
- Bit error rate : Less than 10^{-12} (when a PIONEER optical disk is used)
- Weight : 1.4kg (3 lb, 1 oz)
- Power supply conditions*2 : +5 V, 1.2 A typ, 2.5 A max
  : +12 V, 0.6 A typ, 2.5 A max
- Available positioning : Horizontal or vertical
- Environmental conditions
  Operating temperature : +5°C ~ +40°C (+41°F ~ +104°F)
  Operating humidity : 10% ~ 80% RH (no condensation)
  Storage temperature : –20°C ~ +50°C (–4°F ~ +122°F)
  Storage humidity : 10% ~ 90%RH (no condensation)

- Accessories
  Manual eject screwdriver 1
  Jumper pin 9
  Operating instructions 1

*1 SCSI ..... Small Computer System Interface
*2 The typical value is the value when the drive is not executing a command.

NOTE:
Specifications and design subject to possible modifications without notice, due to improvements.